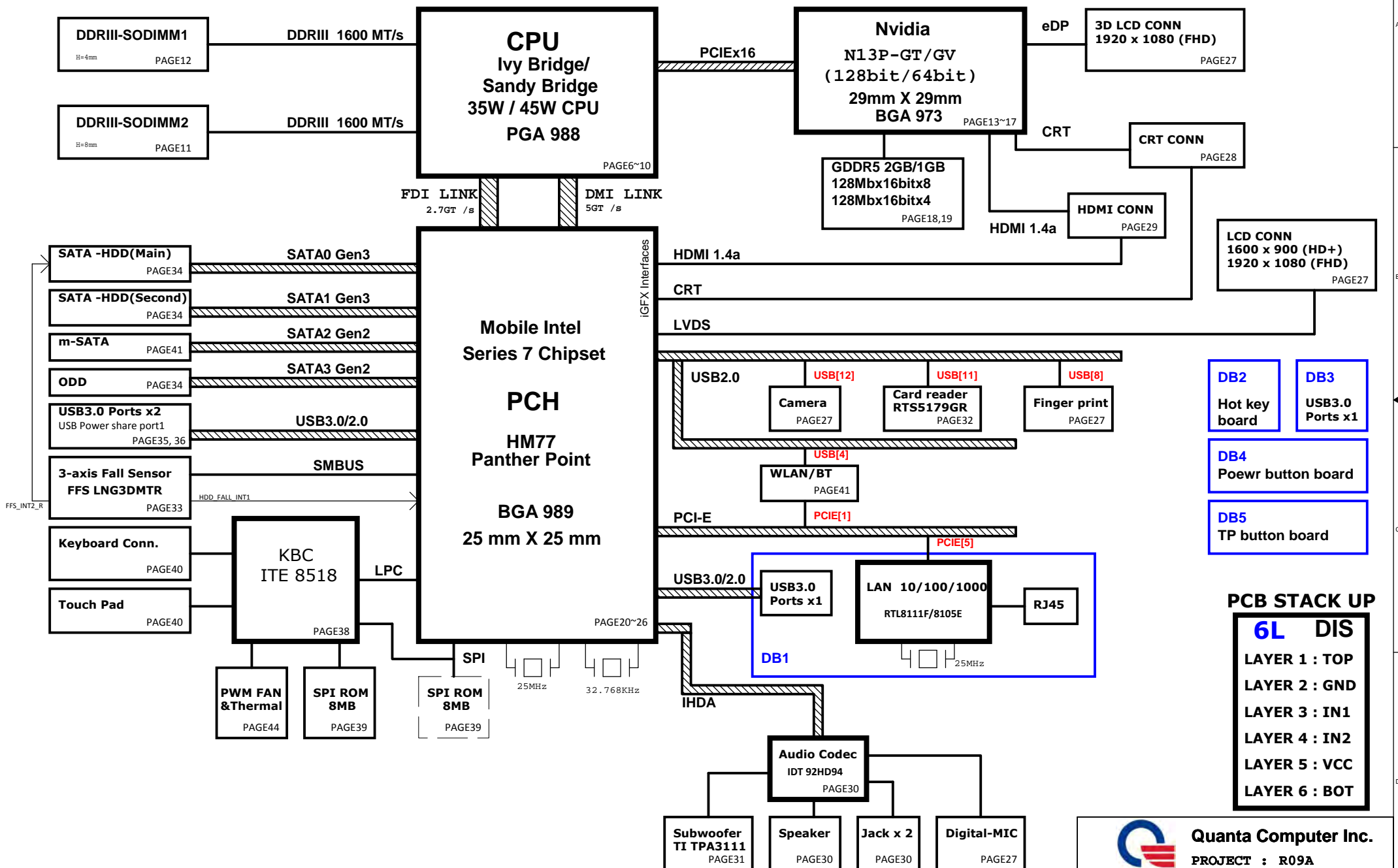
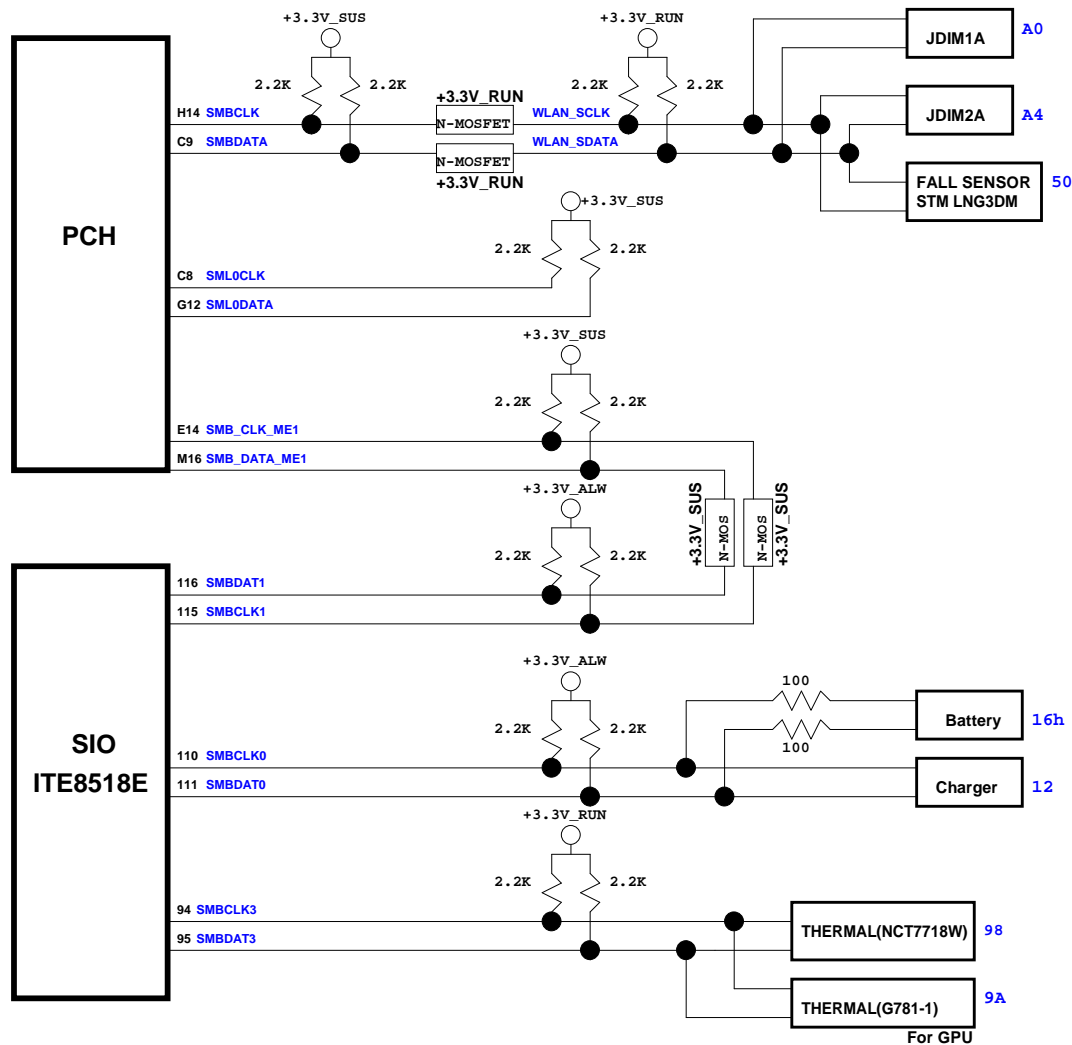


R09/A 17" OPT BLOCK DIAGRAM



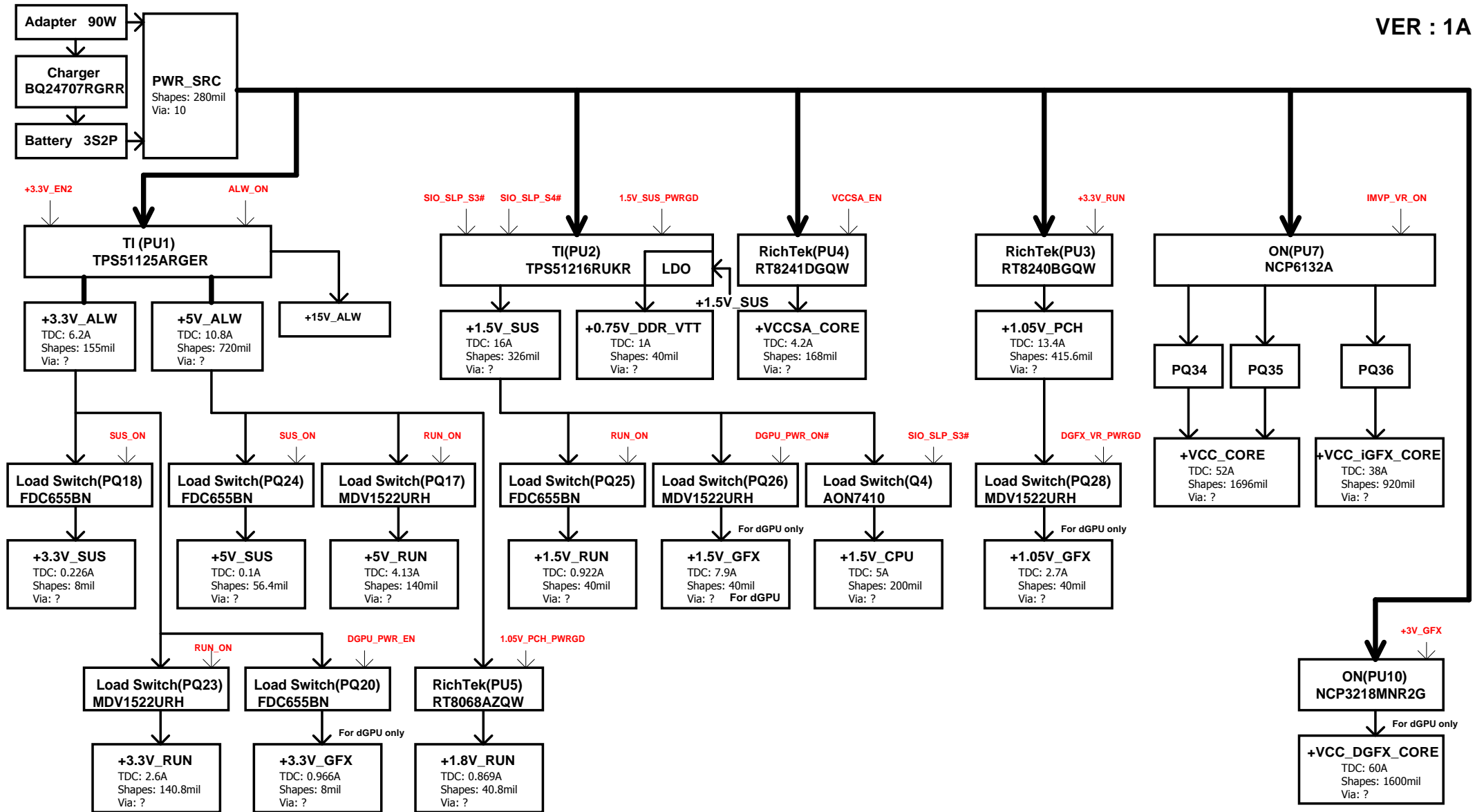


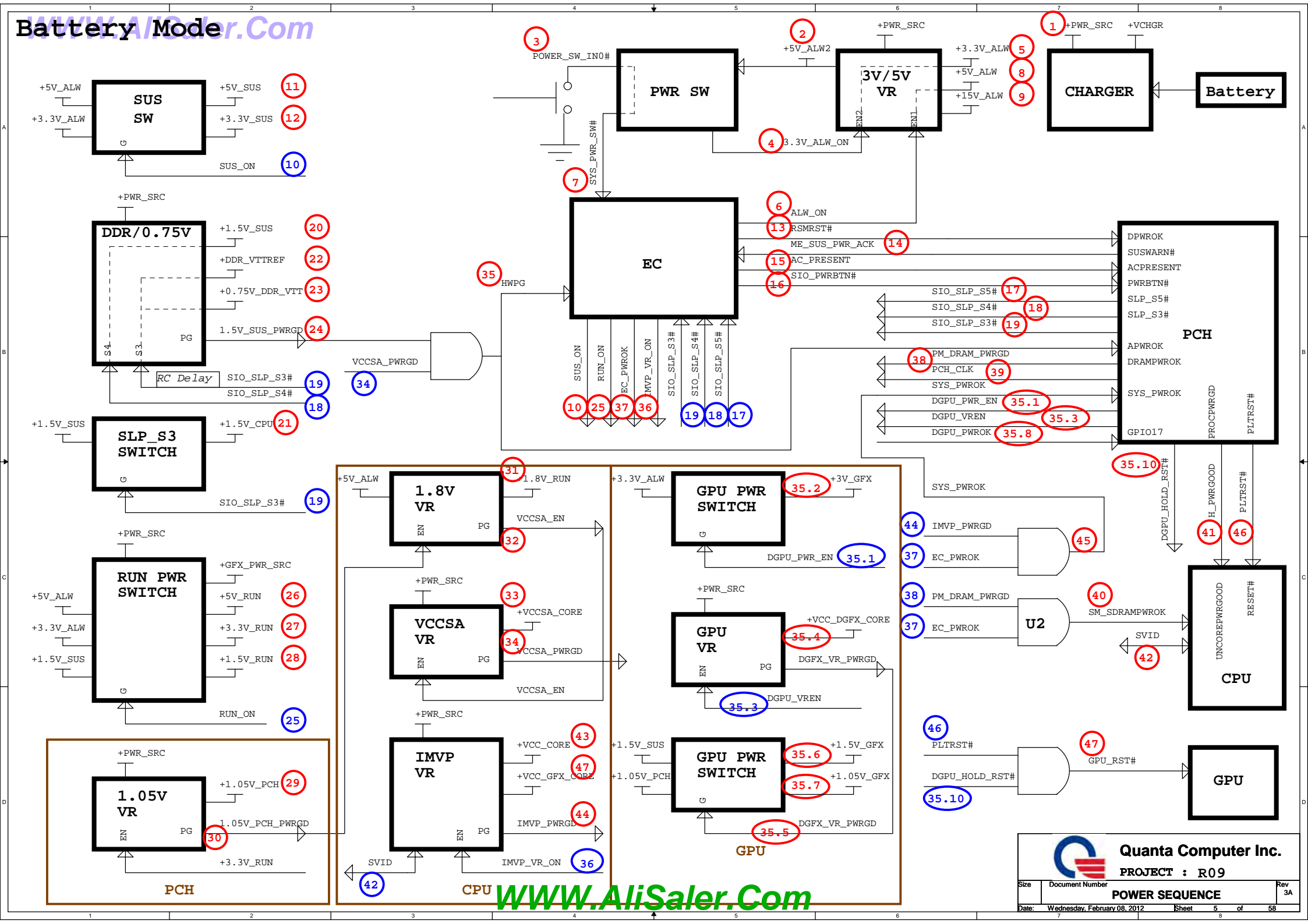
Function	IC	SMBus Address
DDR3	JDIM1A JDIM2A	A0 A4
Thermal IC	G781-1P8 EMC1422	1001101xb (9Ah) 1001100xb (98h)
Charge IC	BQ24707ARGRR	0b00010010 (0x12)
Battery	Battery	16h
Fall Sensor	LNG3DM	01010000 (50h)

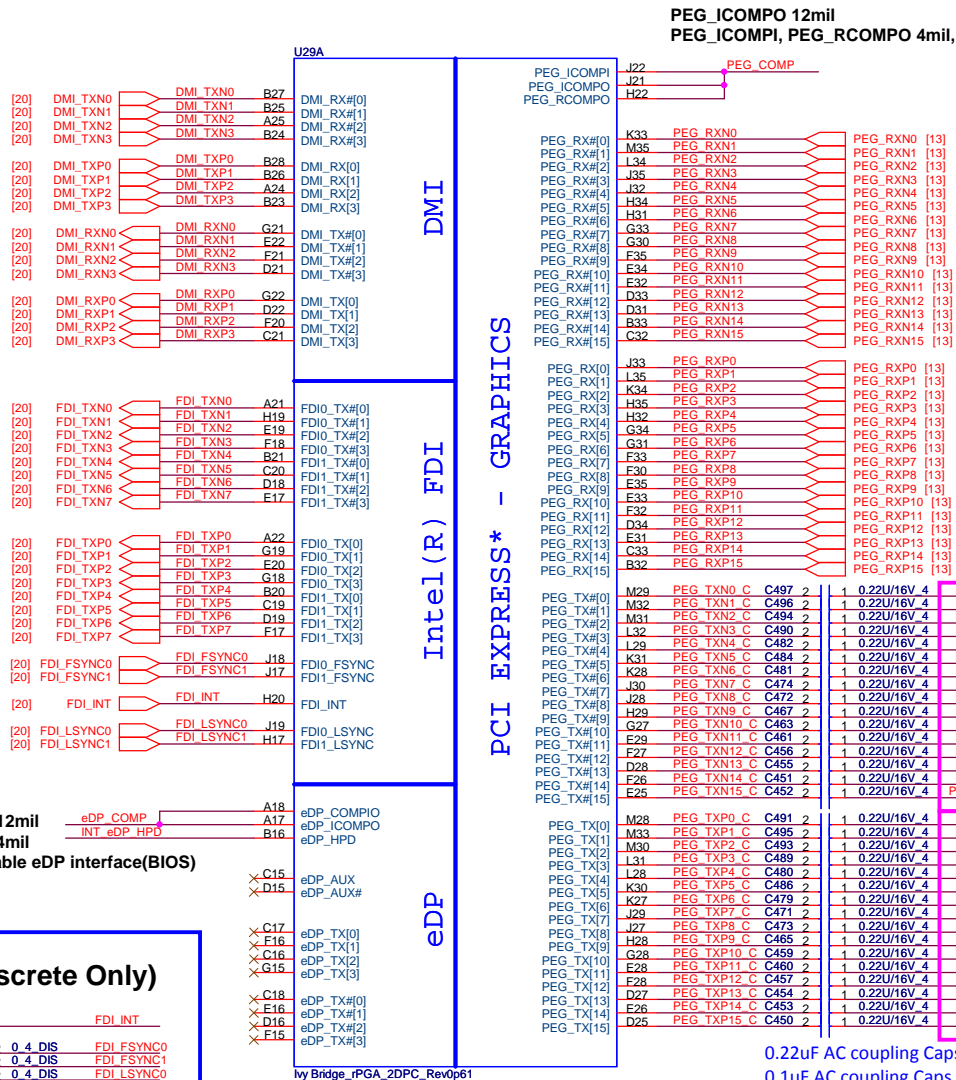
USB Master	Port Assignment
USB0	External port#1 (USB3.0)
USB1	External port#2 (USB3.0 / Power share)
USB2	External port#3 (USB3.0)
USB3	External port#4 (USB3.0)
USB4	MiniCard 1 (WLAN/BT/WiMAX)
USB5	NC
USB6	X(FOR HM77)
USB7	X(FOR HM77)
USB8	Fingerprint
USB9	NC
USB10	Card Reader
USB11	Express Card
USB12	Camera
USB13	NC

SATA Master	Port Assignment
SATA0	HDD Main
SATA1	HDD Second
SATA2	mSATA
SATA3	ODD
SATA4	NC
SATA5	NC

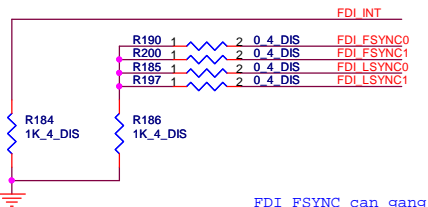
PCIE Master	Port Assignment
PCIE 1	WLAN
PCIE 2	NC
PCIE 3	NC
PCIE 4	NC
PCIE 5	LAN
PCIE 6	NC
PCIE 7	NC
PCIE 8	NC







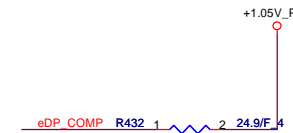
FDI Disabling (Discrete Only)



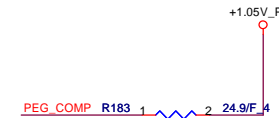
DIS: POP
UMA/ OTP: NC

FDI_FSYNC can gang
all these 4
signals together
and tie them with
only one 1K
resistor to GND
(DG V0.5 Ch2.2.9).

DP & PEG Compensation



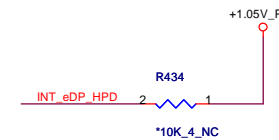
eDP_COMPIO and ICOMPO signals should
be shorted near balls and
routed within 500 mils



PEG_ICOMPI and RCOMPO signals should
be routed within 500 mils

PEG_ICOMPO signals should
be routed within 500 mils

eDP Hot-plug (Disable)



CAD Note: Place PU resistor within 2 inches of CPU

This signal can be left as no connect if entire eDP interface is disabled.

VGA (U3)	AC coupling Cap	PN	TX location	RX location (page13)
N13P-GV	0.1uF CAP CHIP 0.1U 16V(10%,X7R,0402)	CH4103K1B08	C452,C451,C455, C456,C461,C463, C467,C472,C450, C453,C454,C457, C460,C459,C465, C473	C125,C126,C147 C145,C123,C124 C152,C153,C121 C122,C151,C150 C119,C120,C149 C148
N13P-GT	0.22uF CAP CHIP 0.22U 16V(10%,X7R,0402)	CH4223K1B00	ALL	ALL



Quanta Computer Inc.

PROJECT : R09A

Size	Document Number	Rev
	Ivy Bridge 1/5	3A
Date:	Monday, March 05, 2012	Sheet 6 of 58

SNB_IVB# N.A at SNB EDS #27637 0.7v1

[23] H_SNB_IVB# \leftarrow H_SNB_IVB# C26 PROC_SELECT#
[38] H_CPUDET# \leftarrow H_CPUDET# AN34 SKTOCC#

TP1 CATERR# AL33 CATERR#

[38] PECI_EC \leftarrow PECI_EC R159 2 43 4 PECI_EC R AN33 PECI

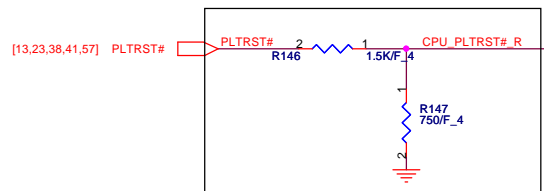
[38,53,55] IMVP7_PROCHOT# \leftarrow IMVP7_PROCHOT# R151 2 56 4 H_PROCHOT# AL32 PROCHOT#

Over 130 degree C will drive low
[25] PM_THRMTRIP# \leftarrow PM_THRMTRIP# AN32 THERMTRIP#

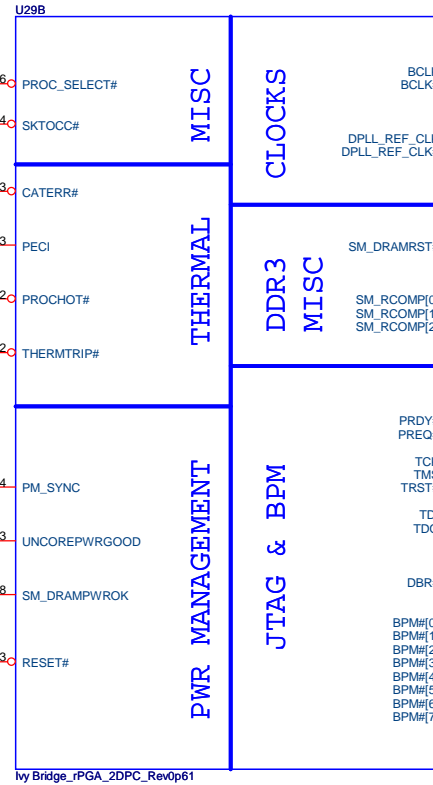
[20] H_PM_SYNC \leftarrow H_PM_SYNC AM34 PM_SYNC

[25] H_PWRGOOD \leftarrow H_PWRGOOD AP33 UNCOREPWRGOOD

10K 4 2 R136 SM_DRAMPWROK V8 SM_DRAMPWROK



Intel spec VinH min =VCCIO X 0.7



Ivy Bridge_rPGA_2DPC_Rev0p61

A28 CLK_CPU_BCLKP [24]
A27 CLK_CPU_BCLKN [24]

A16 CLK_DP_P_R R438 2 1K 4
A15 CLK_DP_N_R R438 2 1K 4 +1.05V_PCH

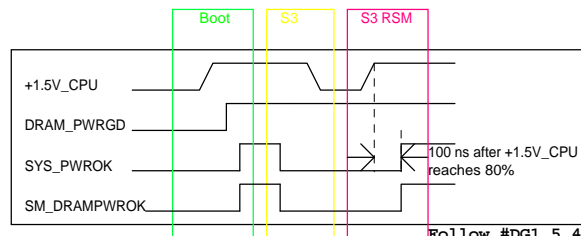
For internal eDP (Disable)

R8 CPU_DRAMRST#
AK1 SM_RCOMP_0 R236 1 2 140F_4
A5 SM_RCOMP_1 R231 1 2 25.5F_4
A4 SM_RCOMP_2 R230 1 2 200F_4
SM_RCOMP_0, SM_RCOMP_1 20mil / SM_RCOMP_2 15mil.

AP29 XDP_TCLK P3
AR27 XDP_TMS P5
AP30 XDP_TRST# P7
AR28 XDP_TDI P6
AP26 XDP_TDO P4
+3.3V_RUN

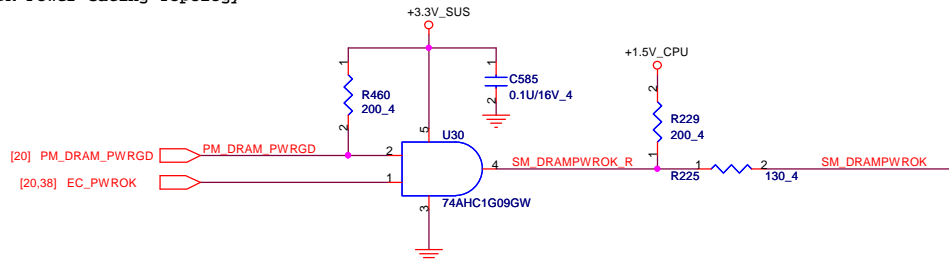
AL35 XDP_DBRST# R152 1 2 1K_4
BPM#[0] AT28
BPM#[1] AR29
BPM#[2] AR30
BPM#[3] AT33
BPM#[4] AP32
BPM#[5] AT31
BPM#[6] AT35
BPM#[7] AR33

+1.05V_PCH
XDP_TMS R142 2 1 *51_4 NC
XDP_TDI R143 2 1 *51_4 NC
XDP_TDO R141 2 1 *51_4 NC
IMVP7_PROCHOT# R139 2 1 62_4
XDP_TCLK R129 1 2 *51_4 NC
XDP_TRST# R144 1 2 *51_4 NC



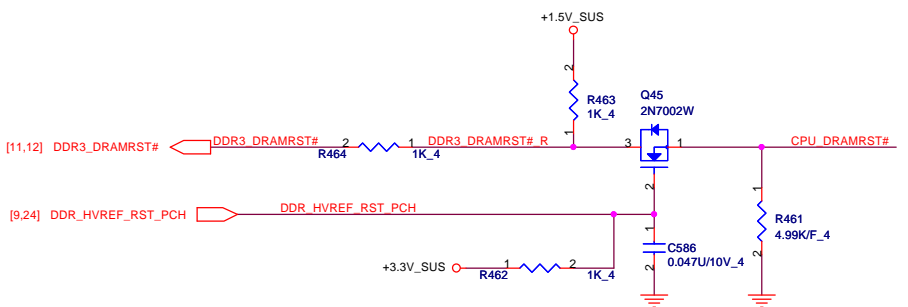
Follow #DG1.5 471984 P119

Follow #DG1.5 471984 P128
DDR Power Gating Topology



when 1,2 is high, 4 is high-impedance OFF-state

Follow #DG1.5 471984 P130
DRAMRST# Routing Illustration



Quanta Computer Inc.
PROJECT : R09A



Ivy Bridge Processor (GRAPHIC POWER)

35W	16pcs
45W	24pcs

CPU Core Power
IVY, SNB: 35W ~ 53A
IVY, SNB: 45W ~ 94A
10F x24

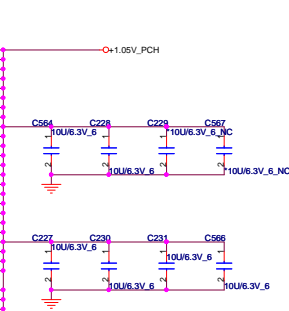
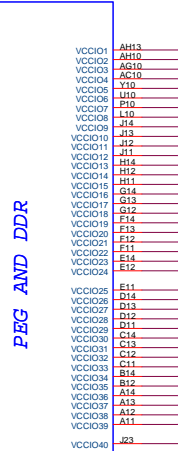
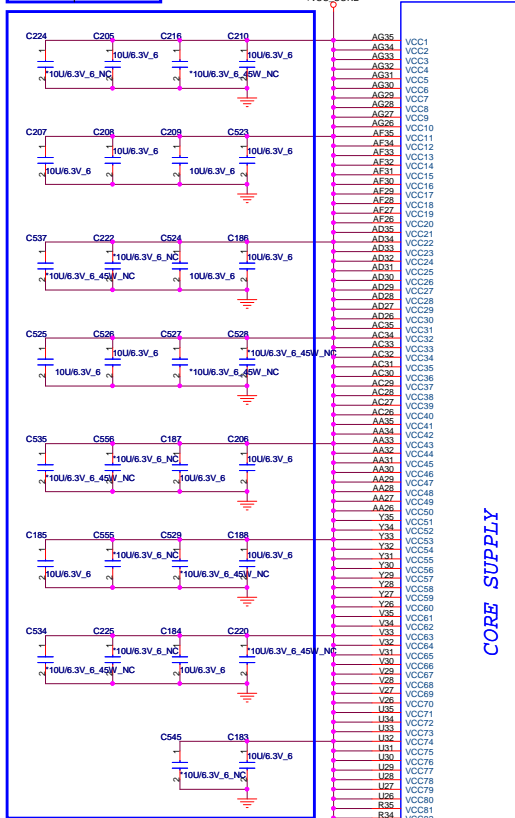
POWER

1.05V_PCH
SNB: 8.5A
IVY: 8.5A
10F x12

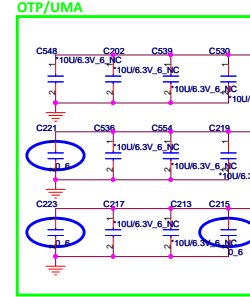
CPU VGT
SNB: 33A
IVY: 33A
10uF x 12

POWER

OTP/UMA: POP
DIS: NC

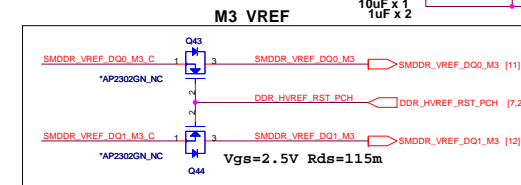


Power Rail Sense Line	R1, R2	Trace Impedance	Trace Length Match
VCC_SENSE / VSS_SENSE	1000	27-330	
VCCA_SENSE / VSSA_SENSE	1000		
VCCIO_SENSE / VSSIO_SENSE	100	550	<25 mils
VCCSA	1000		

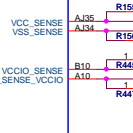


DIS	0 ohm	C221, C223, C215
RESISTOR CHIP	0 1/10W+5%(0603)	
UMA/OPT	C548, C202, C539, C530, C221, C536, C554, C219, C223, C217, C213, C215	
CH6101M9905		
CAP CHIP	10U 6.3V(+20%,X5R,0603)	

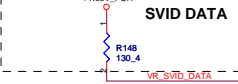
CPU VCCPL
SNB: 1.2A
IVY: 1.2A
10uF x 1
1uF x 2



Vgs=2.5V Rds=115m



Place PU resistor close to CPU



Place PU resistor close to CPU



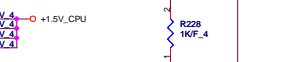
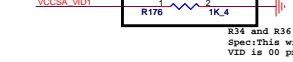
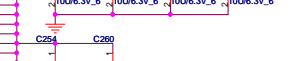
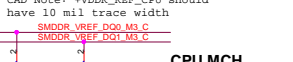
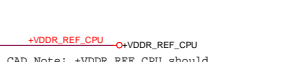
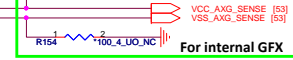
SENSE LINES

VREF

DDR3 - 1.5V RAILS

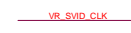
SA RAIL

MISC

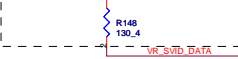


Layout note: need routing together and ALERT need between CLK and DATA

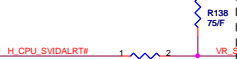
SVID CLK



Place PU resistor close to CPU



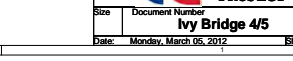
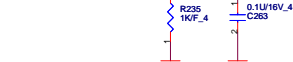
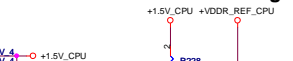
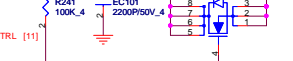
Place PU resistor close to CPU



+5V_ALW



S3 Power reduce



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Ivy Bridge Processor (GND)

Ivy Bridge Processor (RESERVED, CFG)

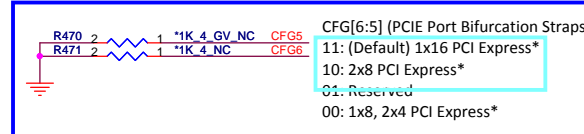
VSS

VSS

CFG

RESERVED

GV - R470 POP
GT, UMA - ALL NC



Processor Strapping

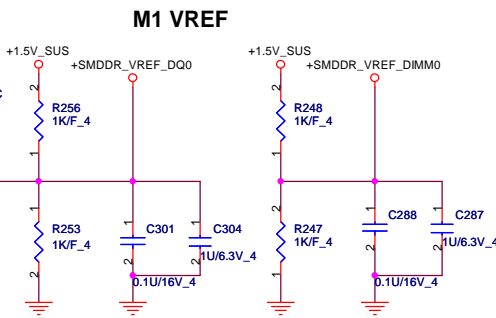
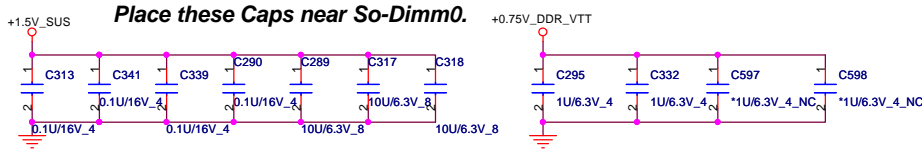
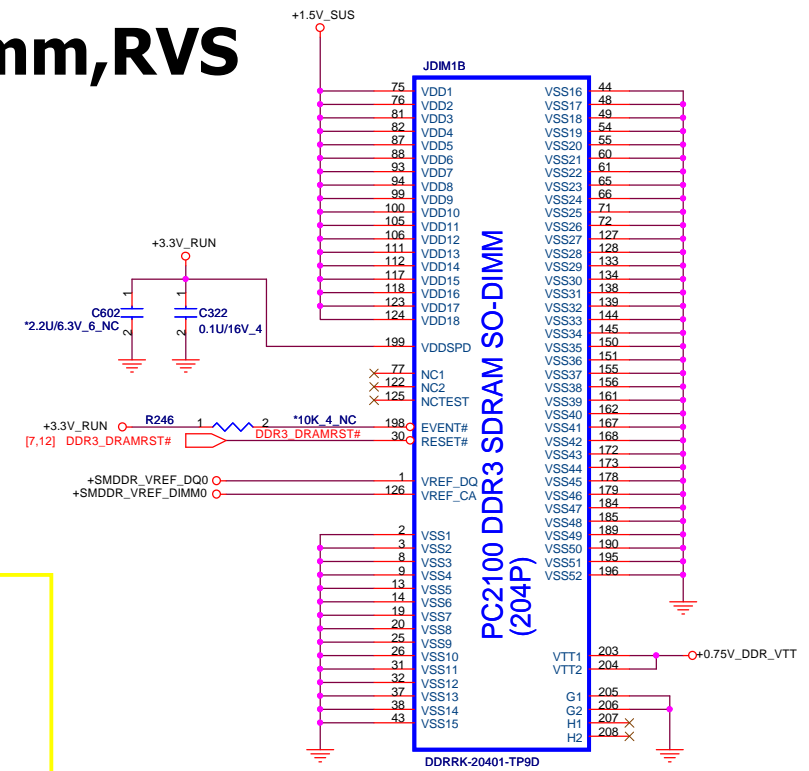
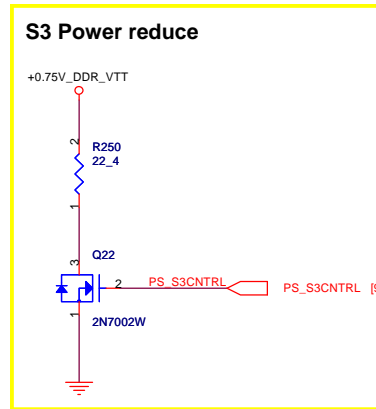
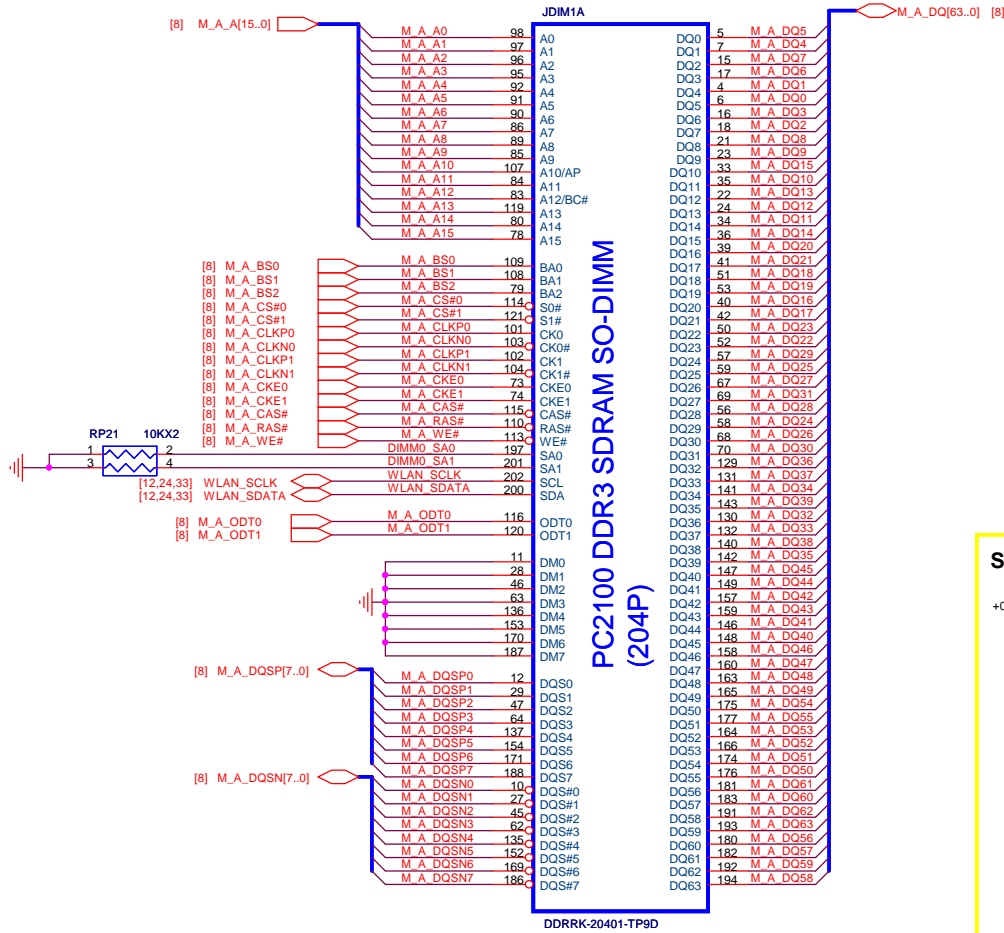
The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PCI-E Static x16 Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP

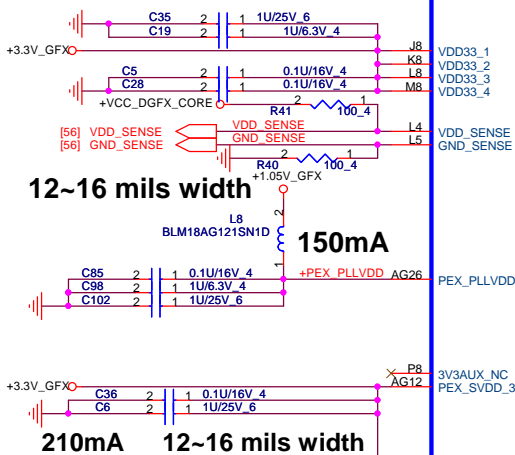
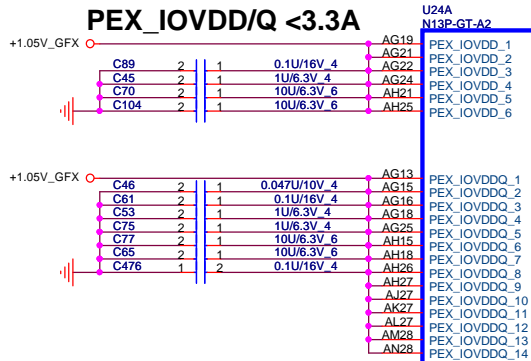
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H=9.2mm,RVS

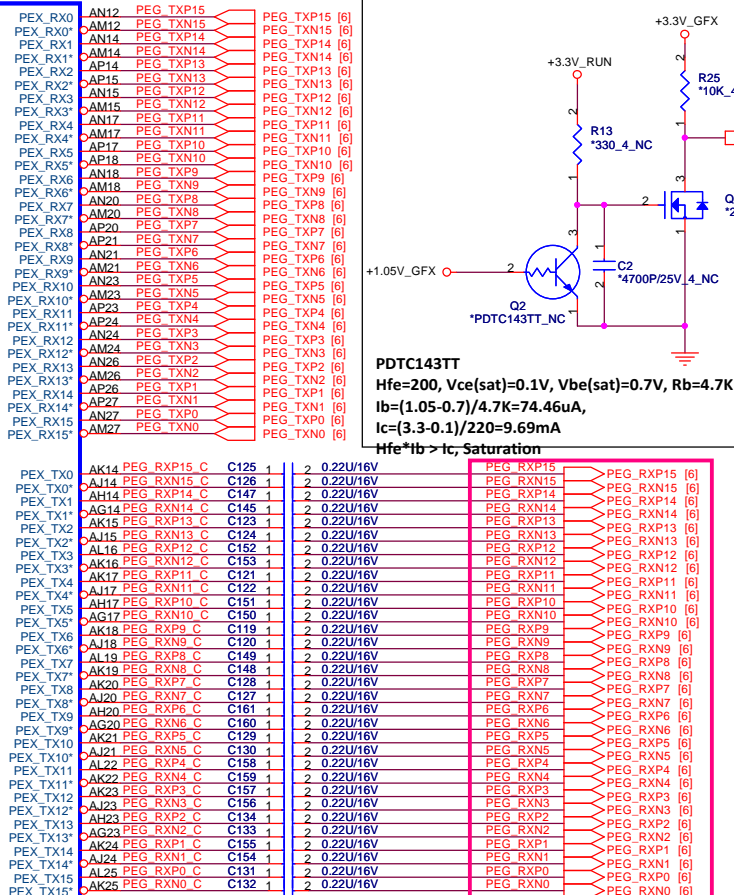


M3 REF

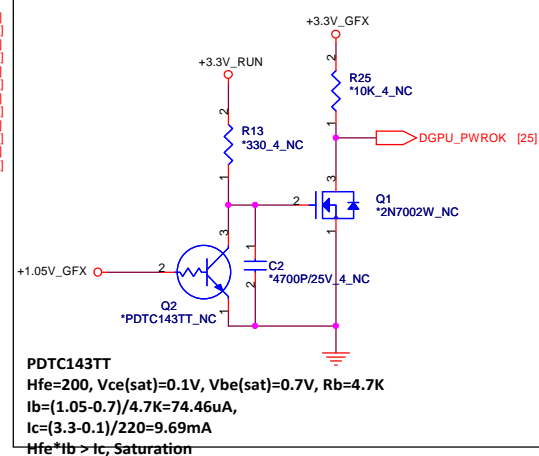


GB4-128

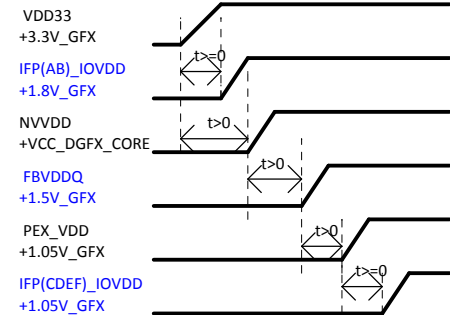
PCI EXPRESS



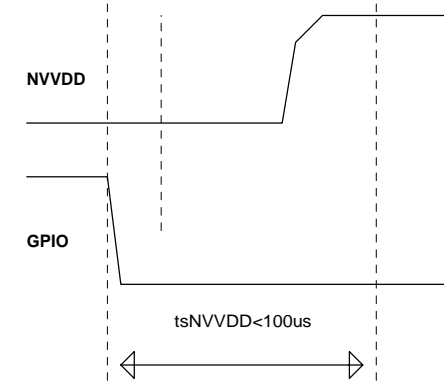
GPU all PWROK



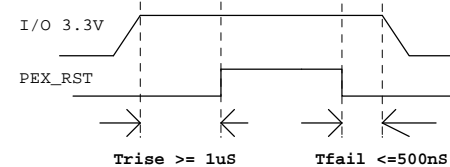
Power up sequence



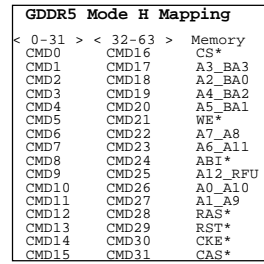
NVVDD Maximum Settling Time



PEX_RST timing

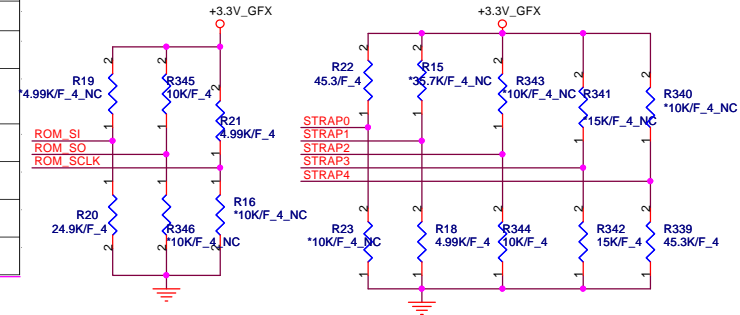


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N13P-GT

	N13P-GT-OPT	N13P-GT-DIS
ROM_SCLK	5K-PU	5K-PU
ROM_SO	10K-PU	10K-PU
ROM_SI	GDDR5 Hynix-128MX16 ⁶ 25K-PD Samsung-128Mx16-30K-PD	GDDR5 Hynix-128MX16 ⁶ 25K-PD Samsung-128Mx16-30K-PD
STRAP-1	5K-PD	5K-PD
STRAP-2	10K-PD	10K-PD
STRAP-3	5K-PD	15K-PD
STRAP-4	45K-PD	45K-PD



N13P-GV

For N13P-GV-B-A2, the n/w strap setting must be modified as below

ROM_SO PD 10K
ROM_SI PD 10K
ROM_SCLK PD 10K
Strap 4 PD 10K

For Hynix 128MX16 GDDR5
Strap 3 PD 10K
Strap 2 PU 10K
Strap 1 PD 10K
Strap 0 PD 10K

For Samsung 128MX16 GDDR5
Strap 3 PD 10K
Strap 2 PU 10K
Strap 1 PD 10K
Strap 0 PD 10K

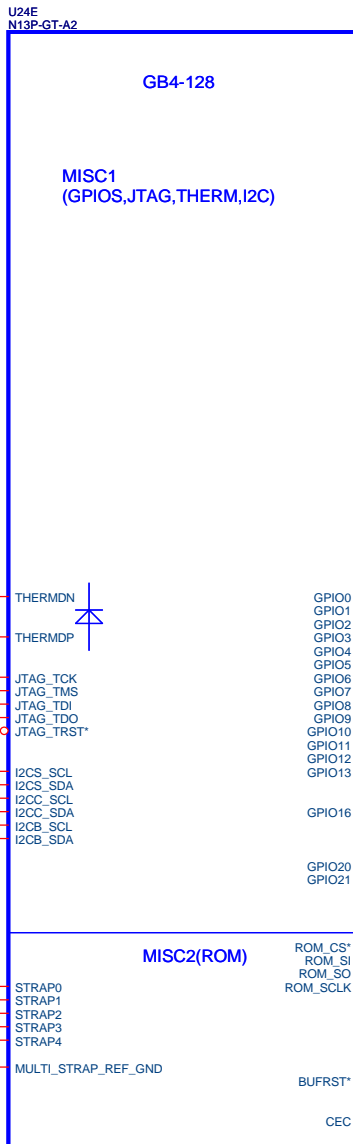
Default: Hynix VRAM (0100) VRAM Configuration Table

RAMCFG [3:0]	DESCRIPTION	Vendor	Quanta P/N	Vendor P/N	ROM_SI
0100	GDDR5 128Mx16, 2500MHz	Hynix	AKG5MWUTW14	H5GQ2H24MFR-T2C	PD 25K
0101	GDDR5 128Mx16, 2500MHz	Samsung	AKG5MWDT509	K4G20325FD-F	PD 30K

SOR_EXPOSED[3:0]		STRAP3
0000	Optimus	PD 5K
0010	Discret only	PD 15K

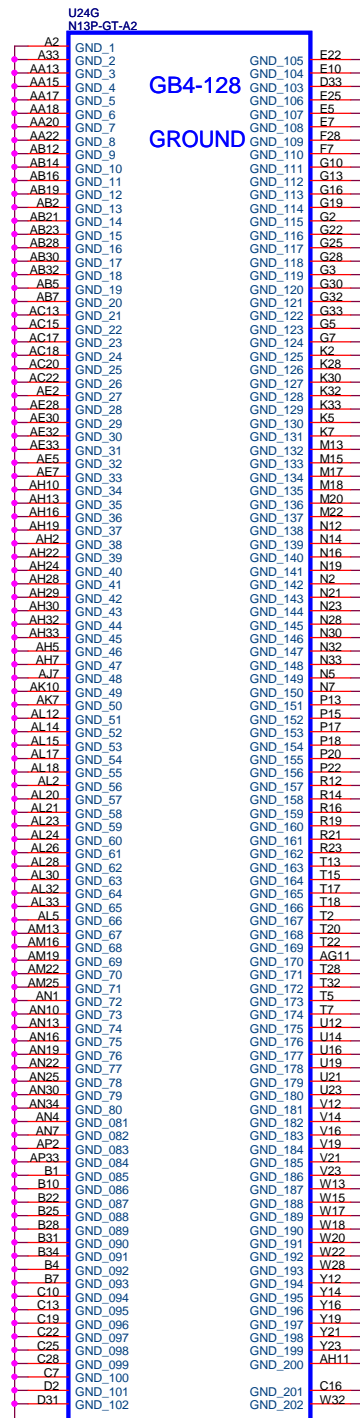
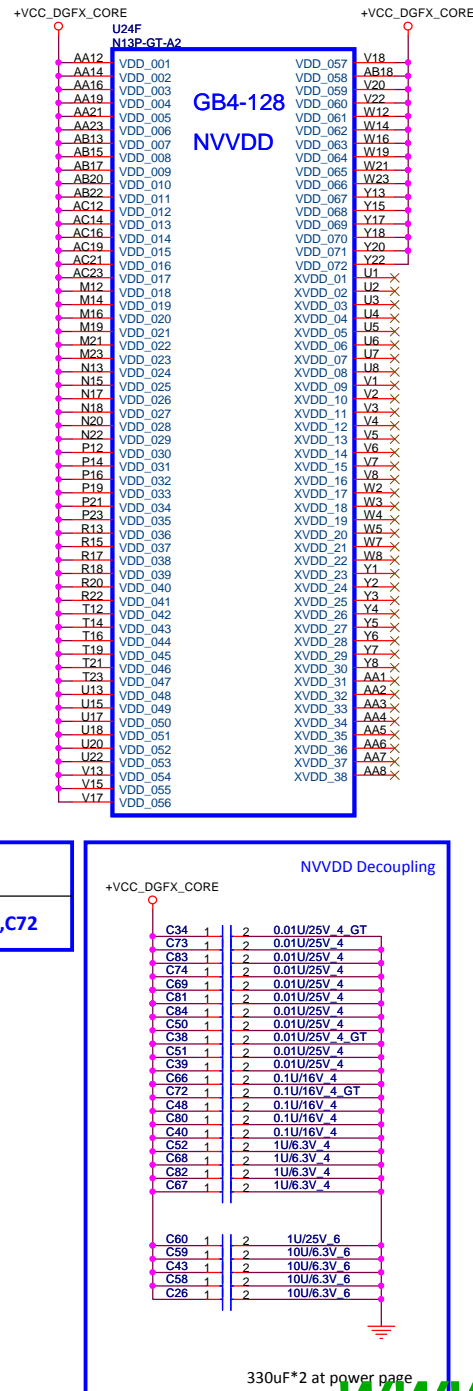
Display configuration table

GPIO	I/O	ACTIVE	USAGE
0	OUT	N/A	NVDD VID4
1	OUT	N/A	NVDD VID3
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVDD VID1
6	OUT	N/A	NVDD VID2
7	OUT	N/A	3D VERSION LEFT/RIGHT SIGNAL
8	I/O	LOW	OVERT
9	I/O	LOW	ALERT
10	OUT	N/A	MEMORY VREF CONTROL
11	OUT	N/A	NVDD VID0
12	IN	N/A	PWR_LEVEL
13	OUT	N/A	NVDD VID5



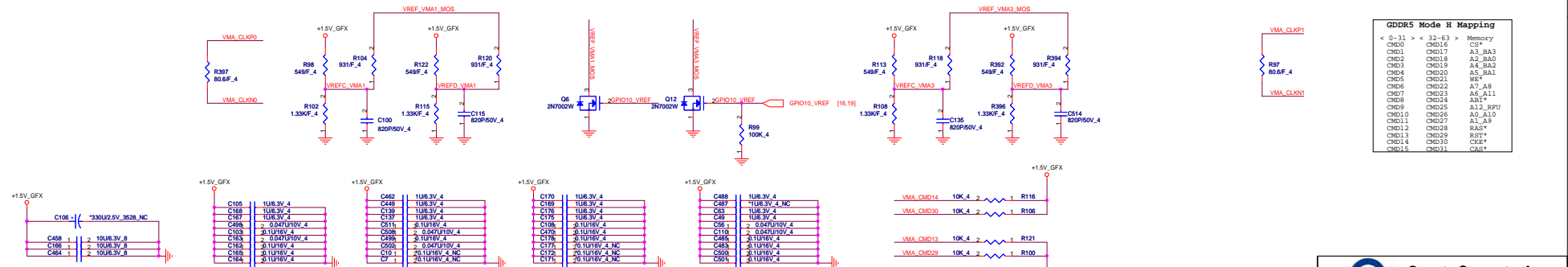
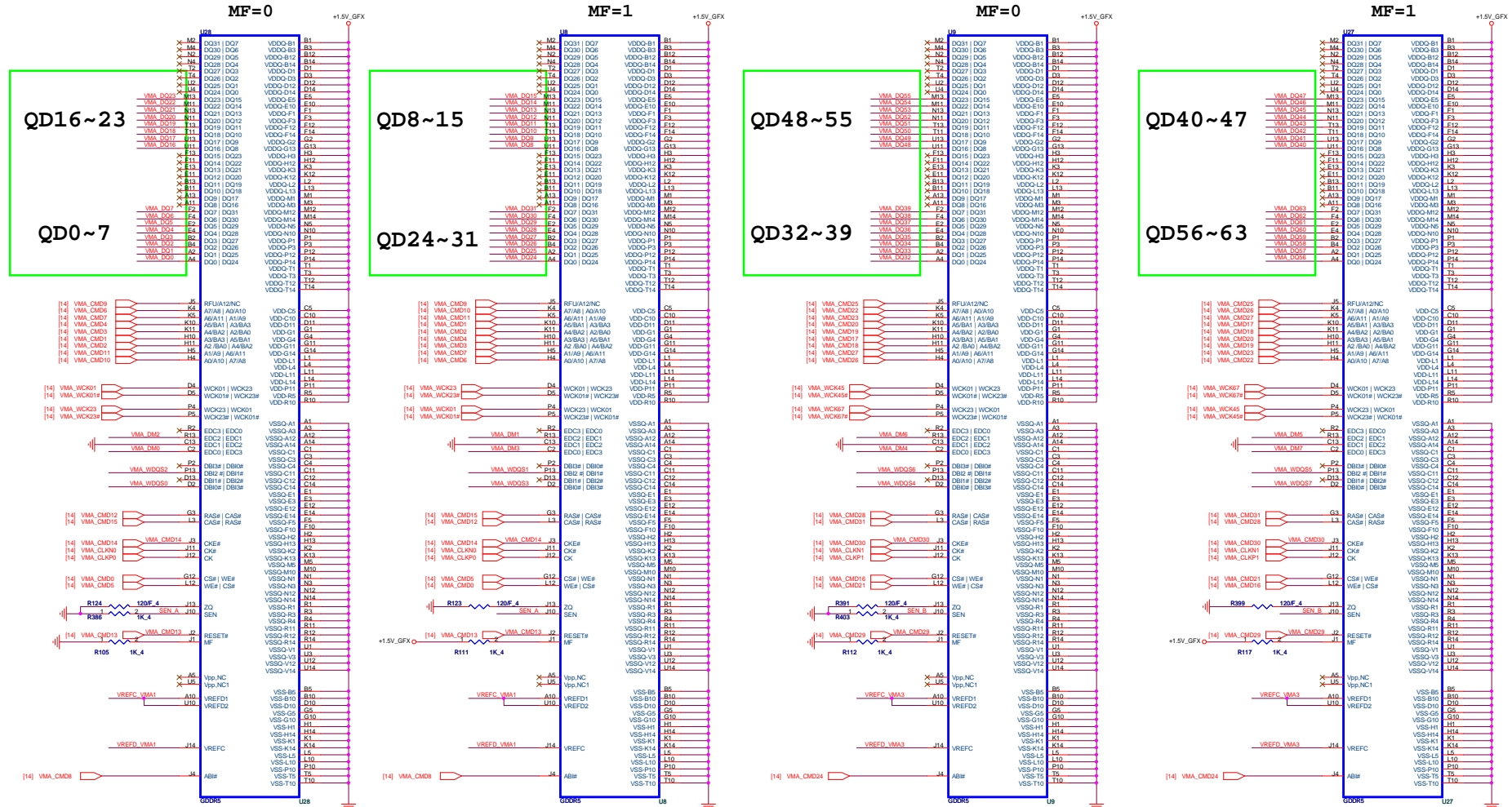
	Output	VID0	VID1	VID2	VID3	VID4	VID5
N13P-GV(QS)	0.875V	0	1	0	0	1	1
N13P-GT(QS)	0.9V	0	0	0	0	1	1

GT: 60A	all POP
GV: 42A	NC C34,C38,C72



LOWER HALF

UPPER HALF



GDDR5 Mode H Mapping		
< 0-31	< 32-63	Memory CS*
CM01	CM016	A3_BA3
CM02	CM017	A2_BA0
CM03	CM018	A4_BA2
CM04	CM020	A5_BA1
CM05	CM021	WE*
CM06	CM022	A7_A8
CM07	CM023	A6_A11
CM08	CM024	AB1*
CM09	CM025	A12_RFU
CM10	CM026	A0_A10
CM11	CM027	A1_A9
CM12	CM028	RA*
CM13	CM029	RST*
CM14	CM030	CKE*
CM15	CM031	CAS*

LOWER HALF

UPPER HALF

MF=0

MF=1

MF=0

MF=1

QD16~23

QD0~7

QD8~15

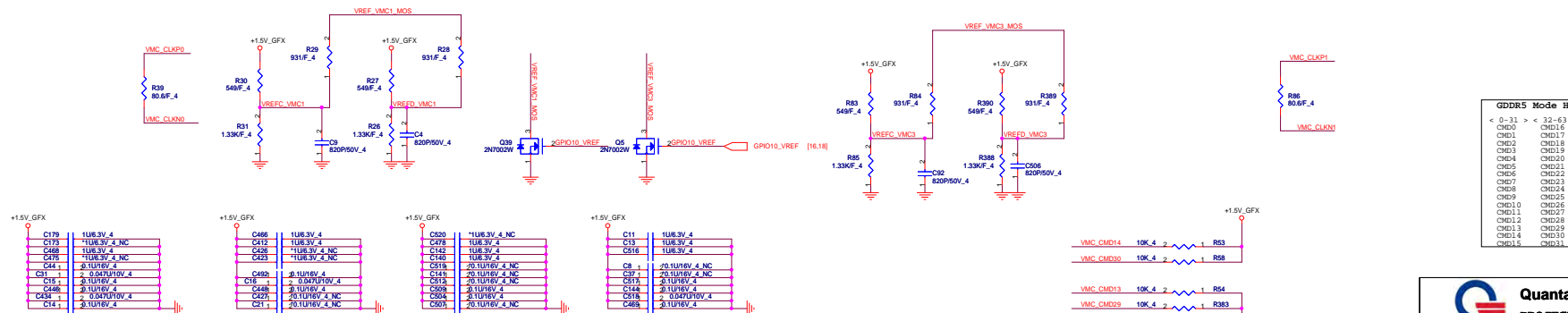
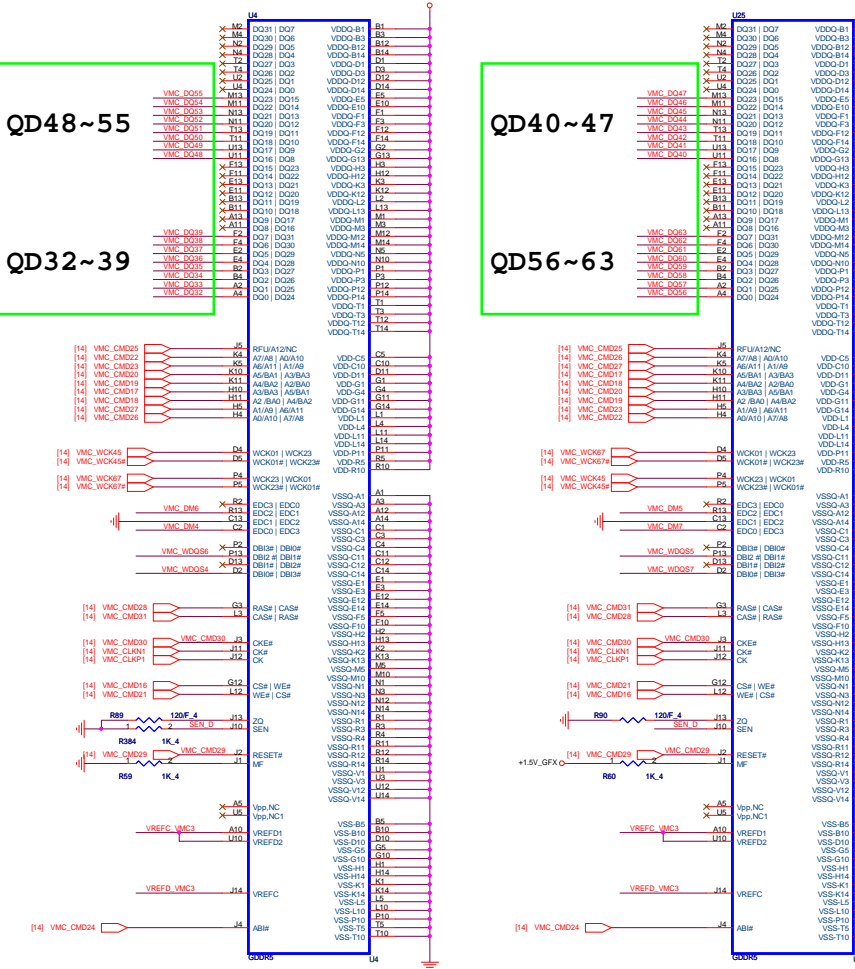
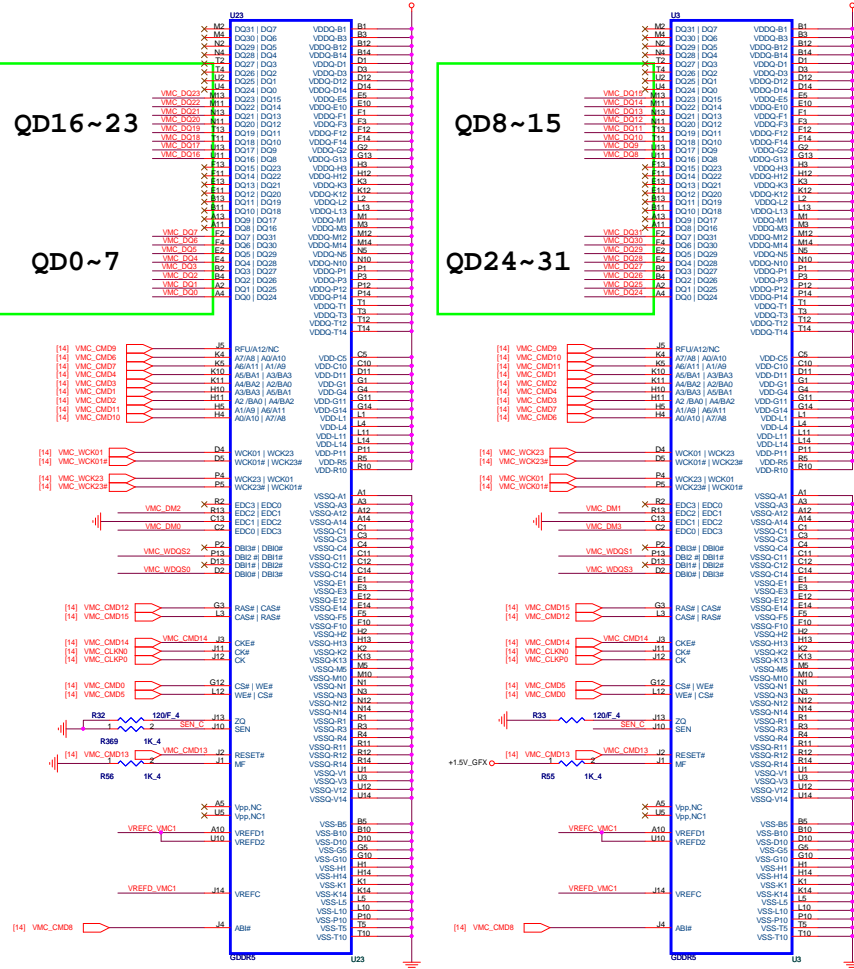
QD24~31

QD48~55

QD32~39

QD40~47

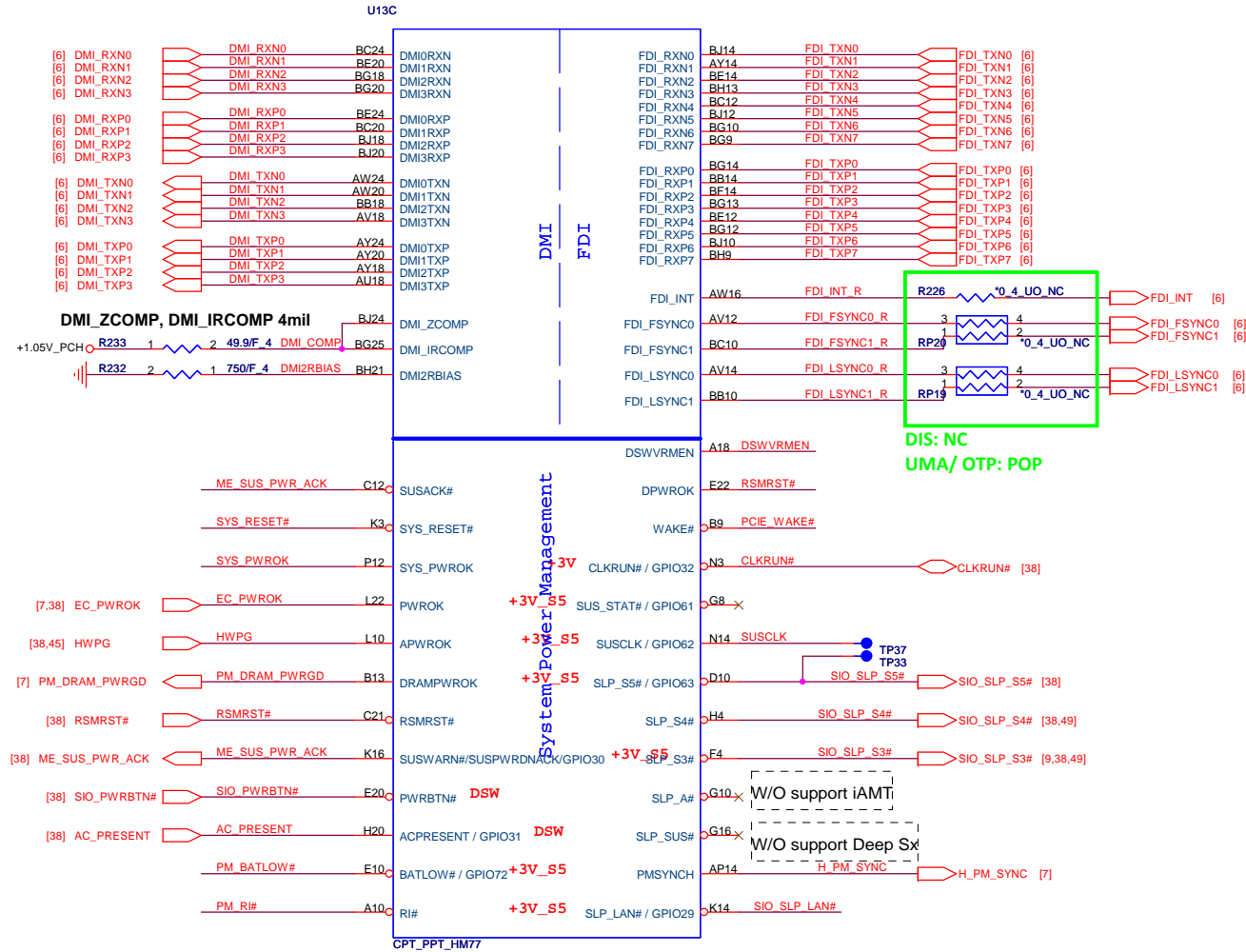
QD56~63



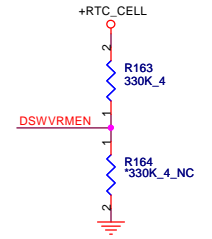
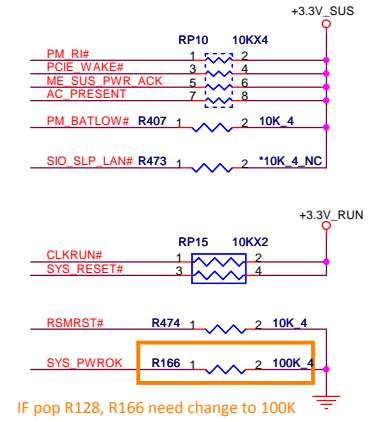
GDDR5 Mode H Mapping

< 0-31 >	< 32-63 >	Memory
CM016	CM016	CS*
CM017	CM017	A2_BA3
CM018	CM018	A2_BA0
CM019	CM019	A2_BA2
CM020	CM020	A5_BA1
CM021	CM021	WE*
CM022	CM022	A7_A8
CM023	CM023	A6_A11
CM024	CM024	A7_A10
CM025	CM025	A12_RPU
CM026	CM026	A12_A10
CM027	CM027	A1_A9
CM028	CM028	RS*
CM029	CM029	RS*
CM030	CM030	CS*
CM031	CM031	CS*

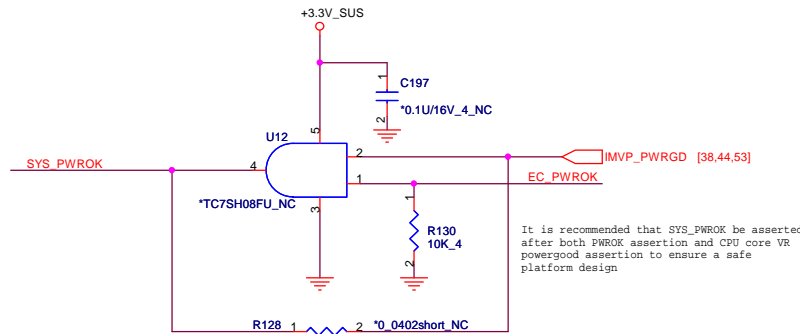
Cougar Point/Panther Point (DMI, FDI, PM)

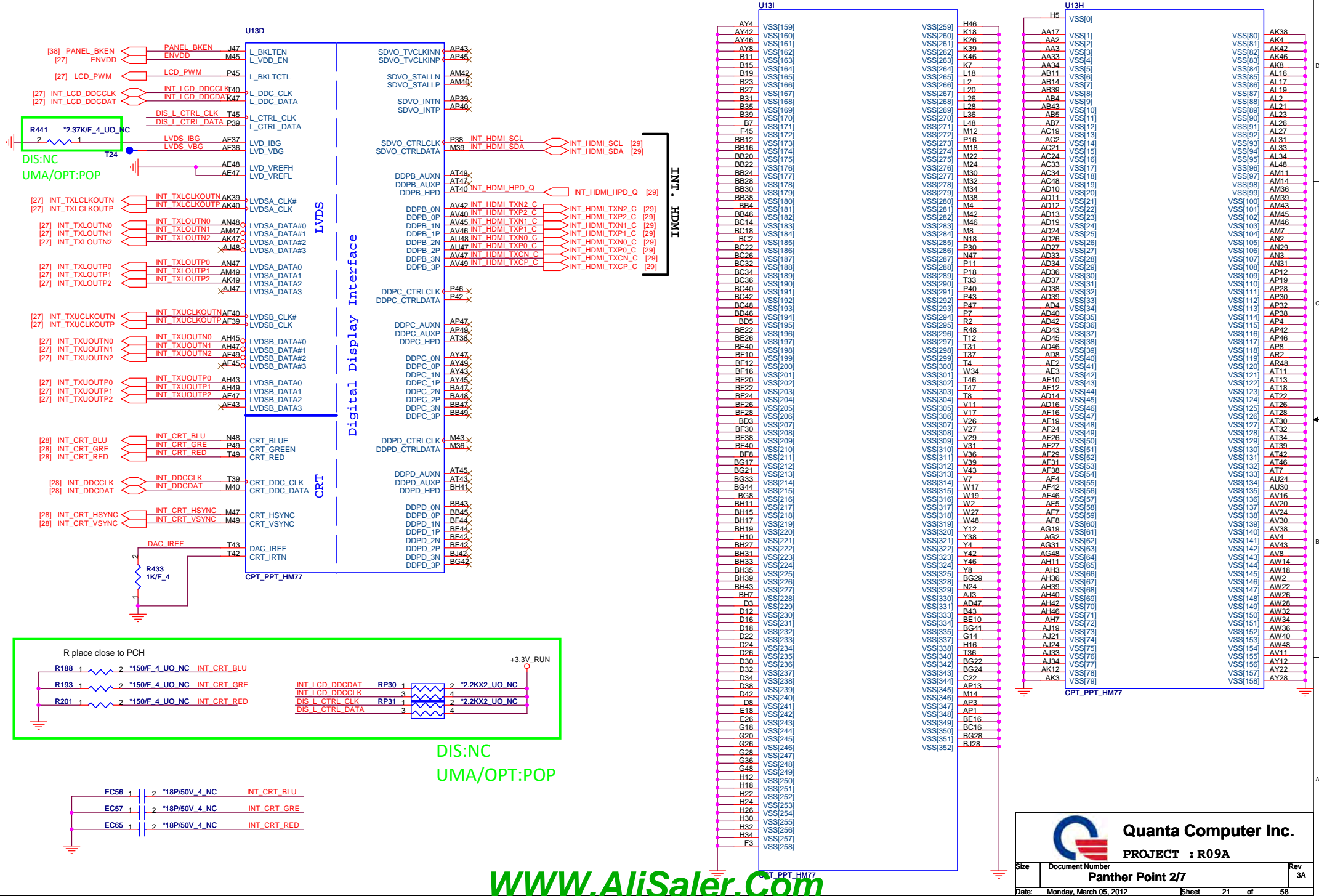


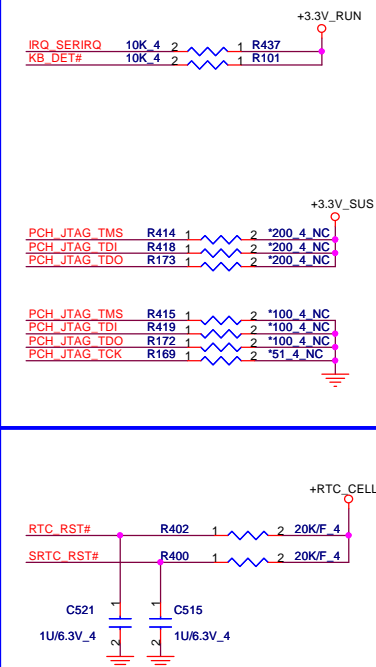
PCH Pull-high/low(CLG)







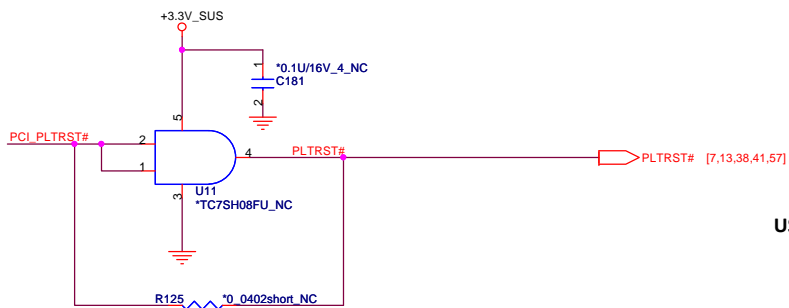
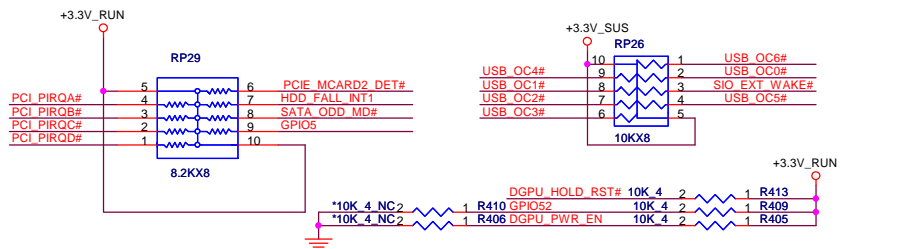
On Die DSW VR Enable
High = Enable (Default)
Low = Disable



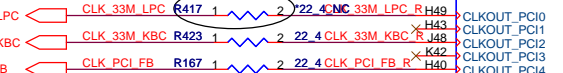
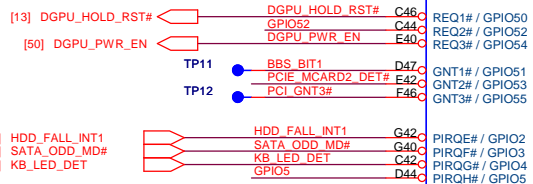
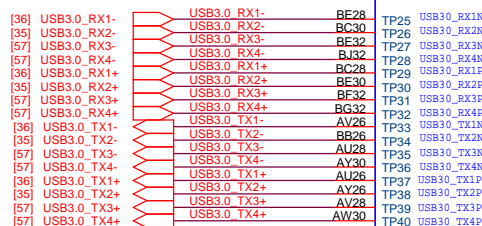




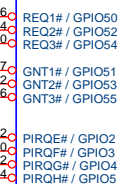
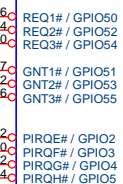
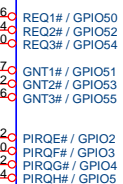
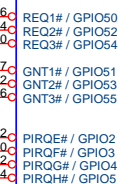
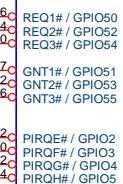
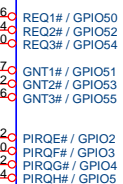
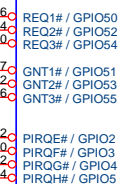
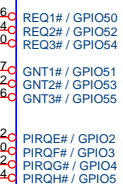
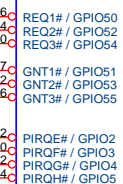
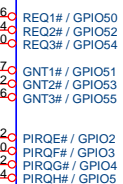
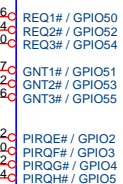
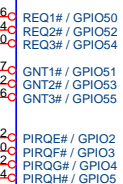
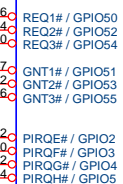
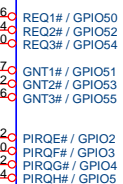
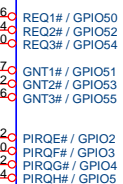
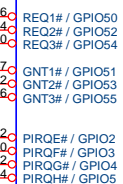
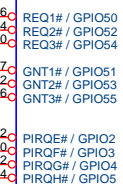
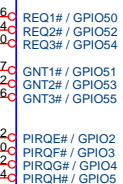
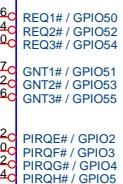
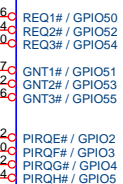
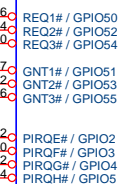
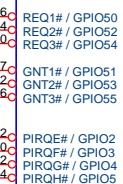
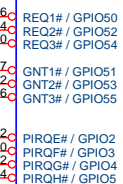
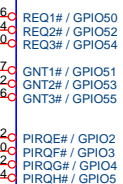
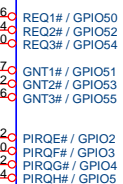
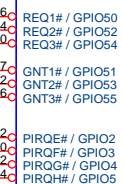
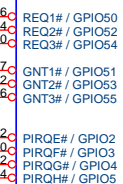
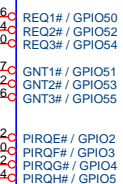
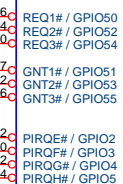
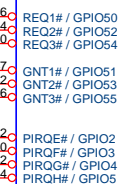
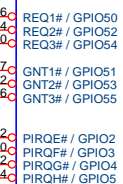
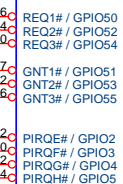
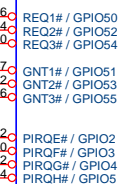
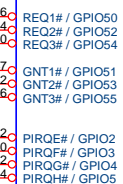
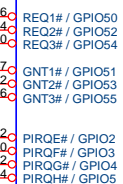
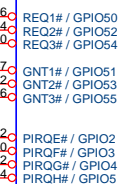
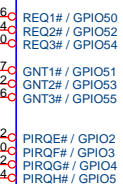
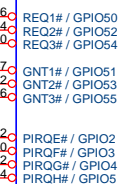
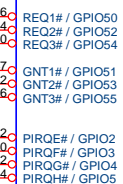
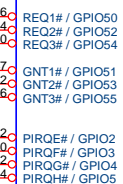
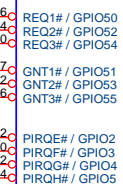
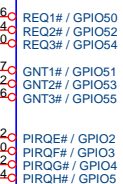
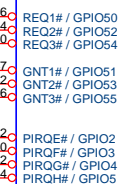
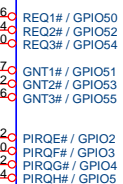
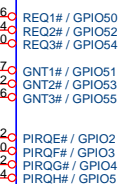
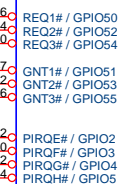
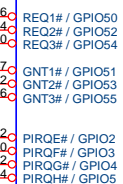
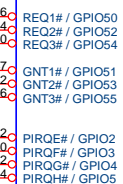
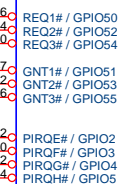
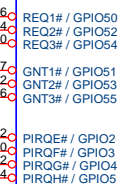
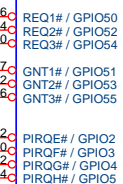
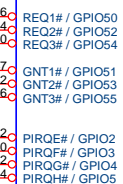
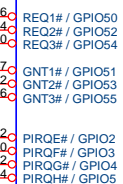
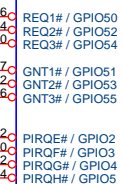
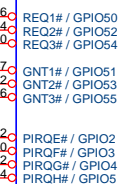
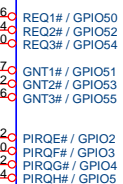
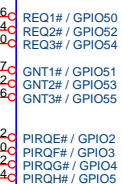
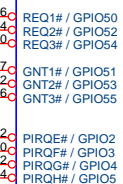
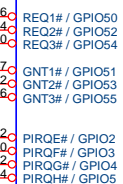
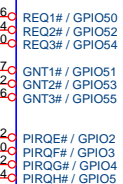
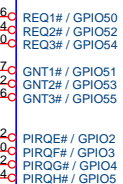
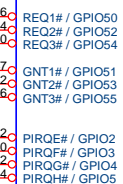
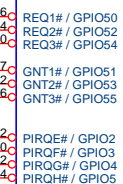
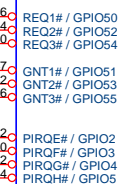
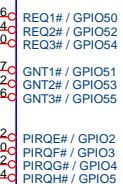
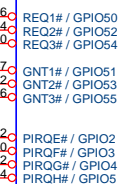
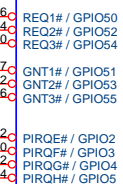
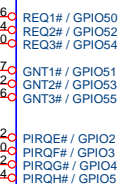
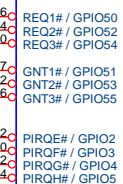
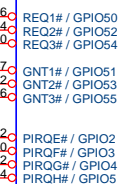
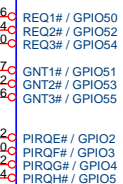
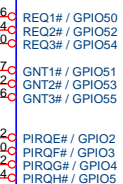
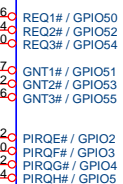
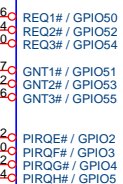
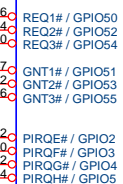
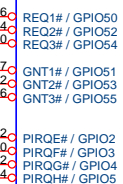
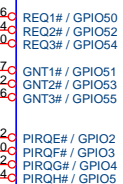
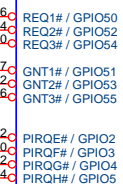
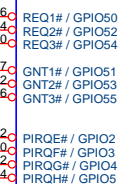
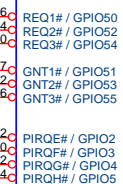
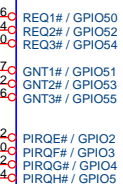
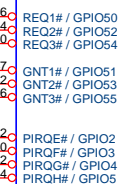
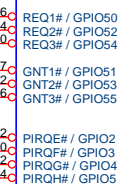
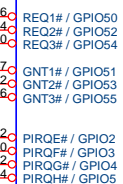
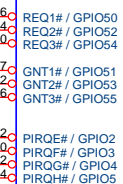
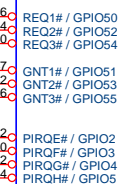
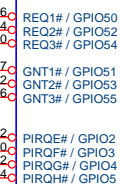
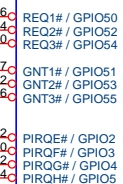
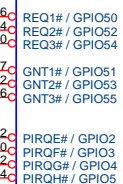
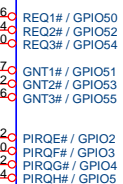
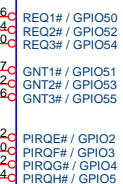
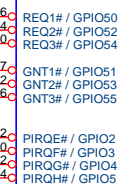
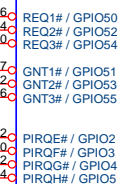
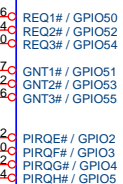
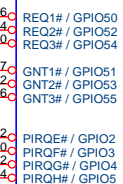
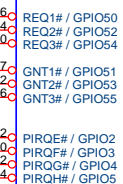
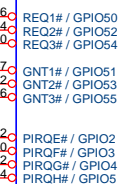
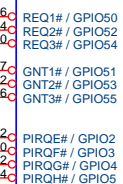
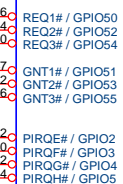
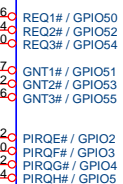
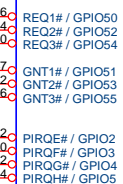
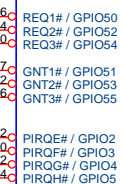
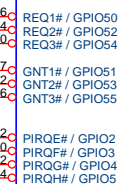
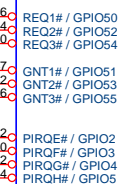
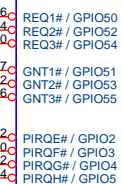
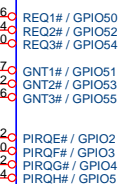
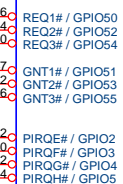
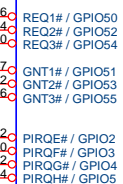
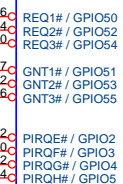
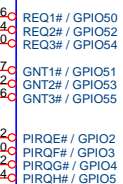
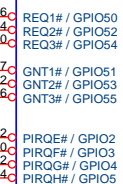
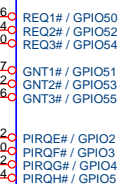
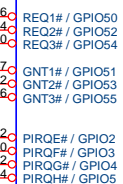
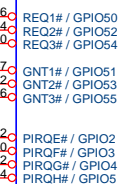
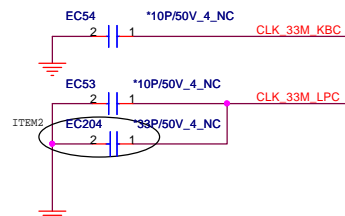
Pin Name	Strap description	Sampled	Configuration	Note
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	NC
HDA_SDO	Flash Descriptor Security	PWROK	0 = Default (weak pull-down 20K) 1 = Override	NC
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+RTC_CELL  R162 1  2 330K 4 PCH_INTVRMEN
HDA_SYNC	On-Die PLL VR Volatge Select	RSMRST	0 = Support by 1.8V (weak PD) 1 = Support by 1.5V	+3.3V_SUS  R134 1  2 1K 4 ACZ_SYNC_R

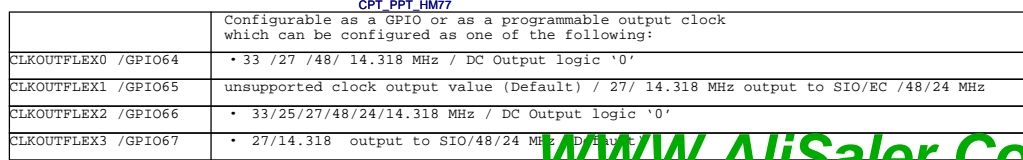


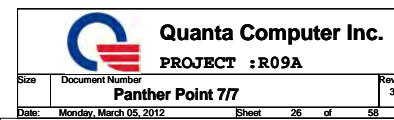
USB3.0

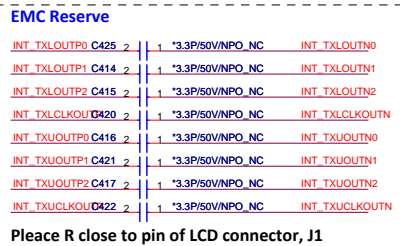
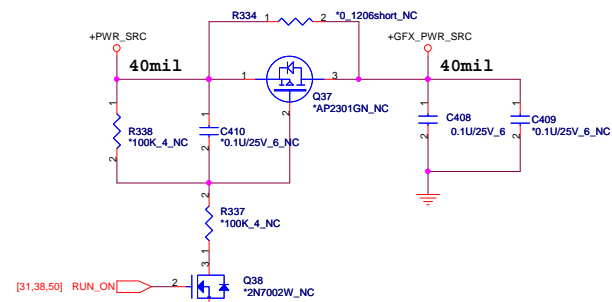
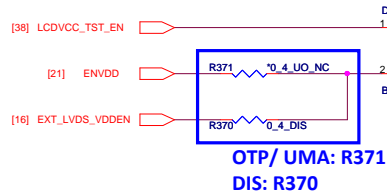
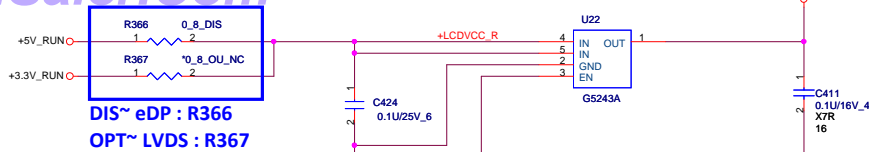


CPT_PPT_HM77

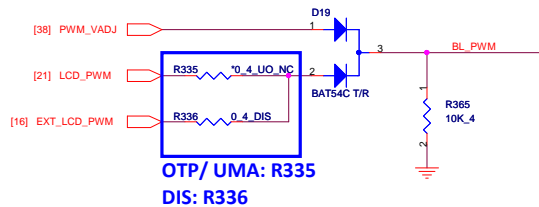




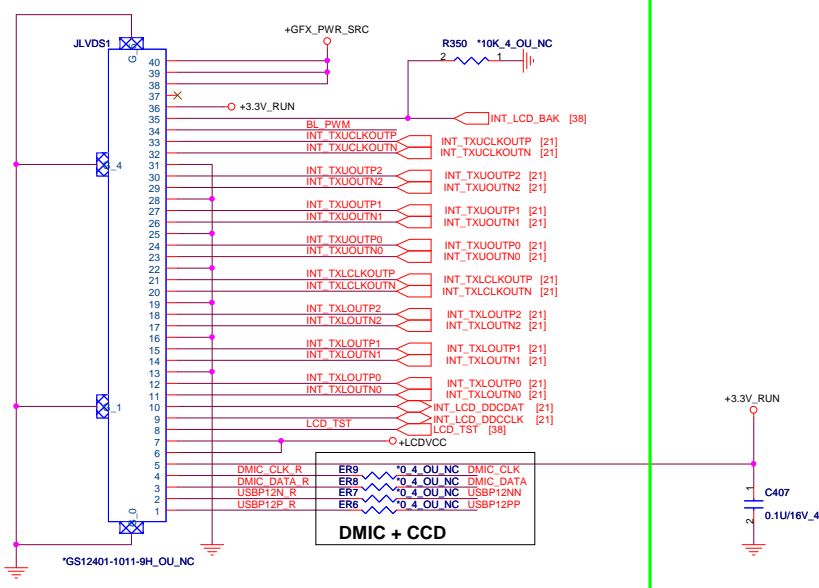




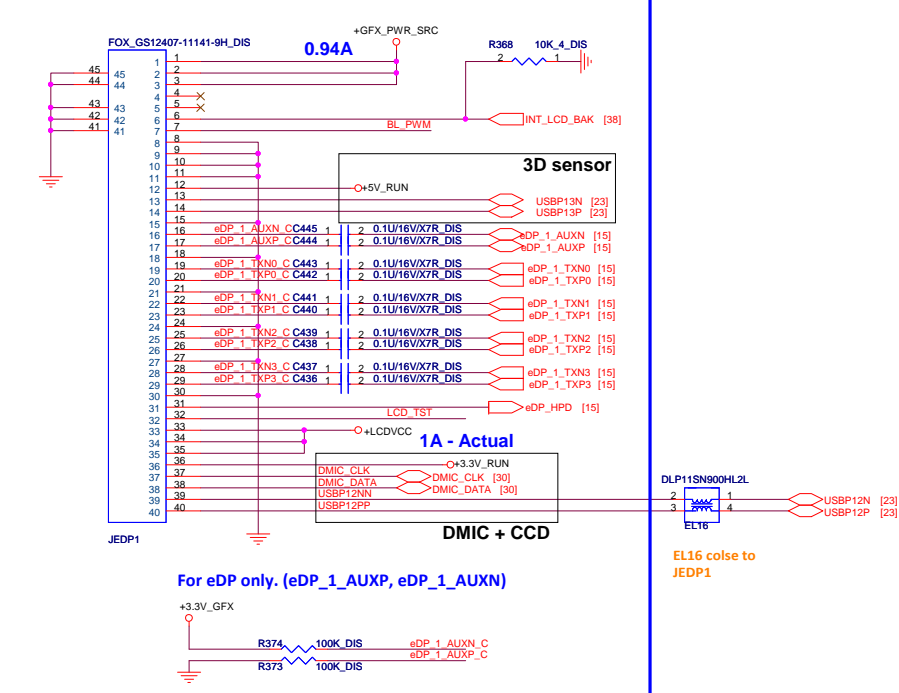
Backlight Control

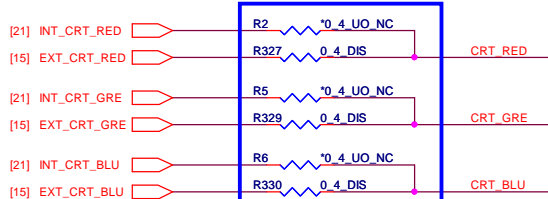


Normal Panel - 40pin

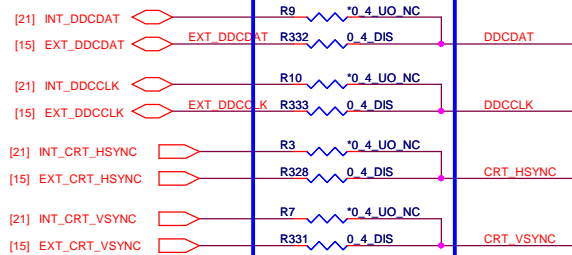


3D Panel - DIS turbo - 40pin



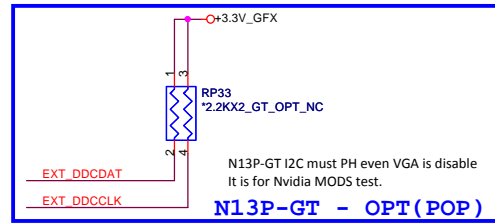
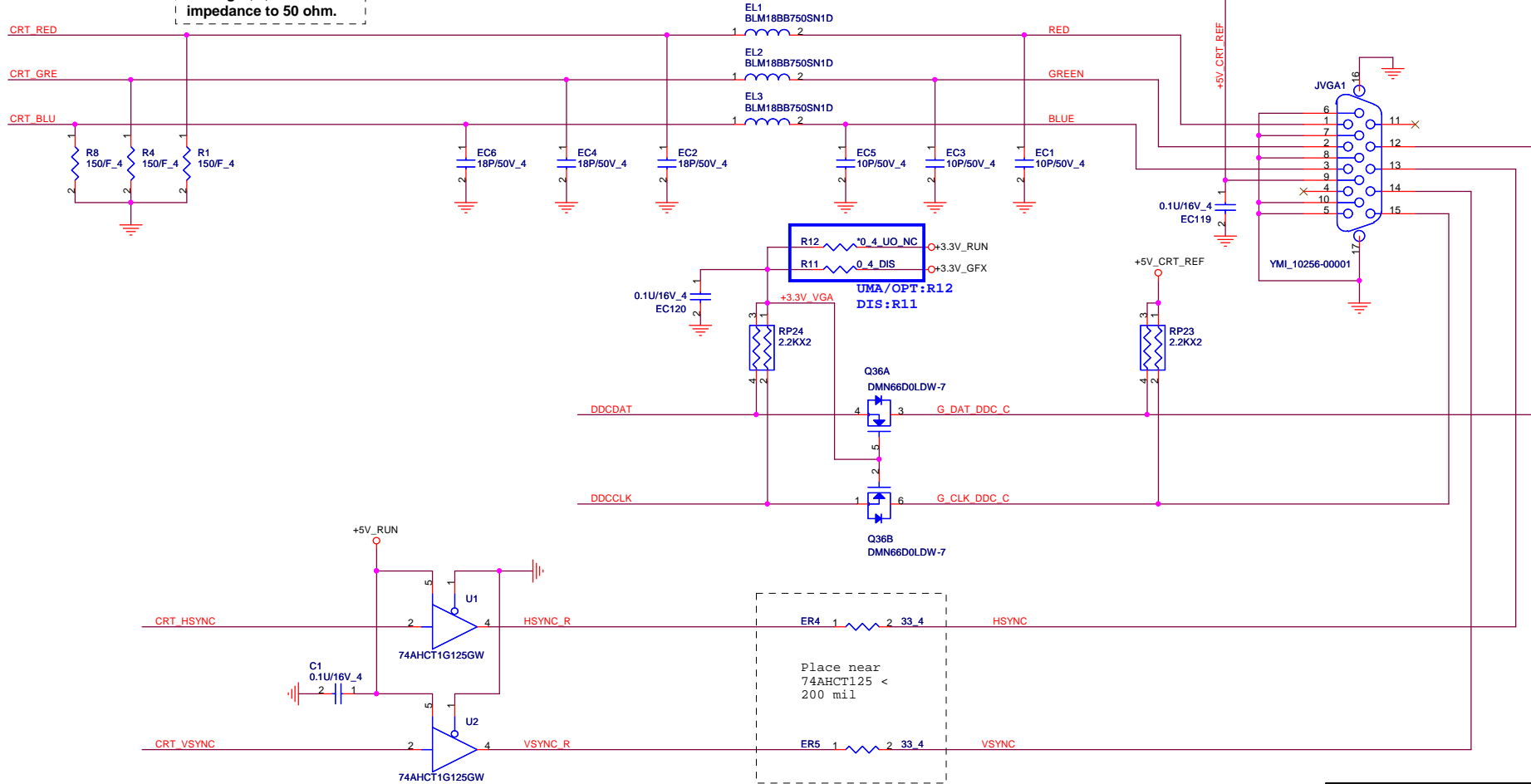


DIS: EXT POP
UMA/OPT: INT POP

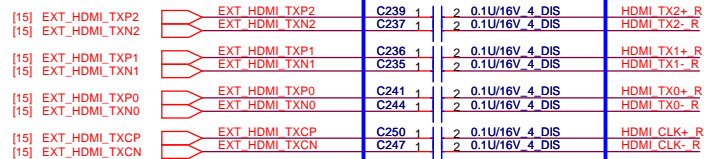


DIS: EXT POP
UMA/OPT: INT POP

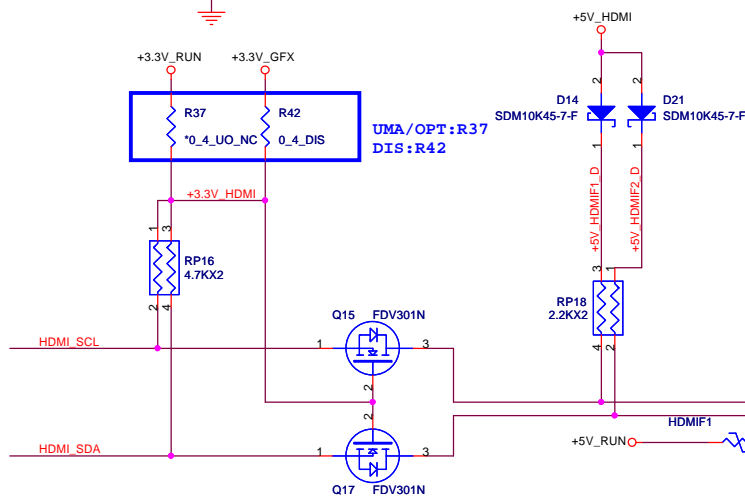
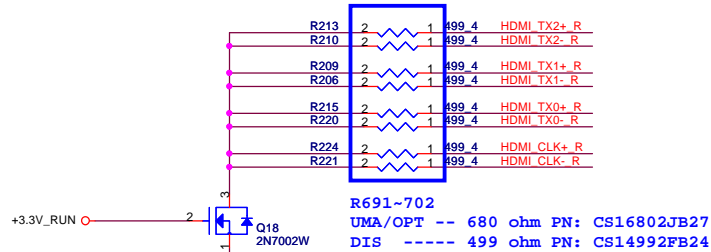
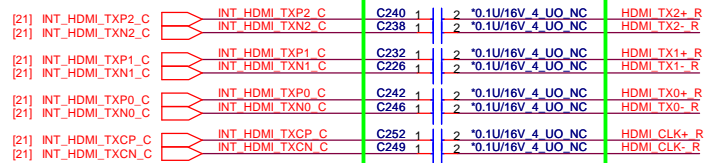
Layout Note:
Setting R,G,B treac
impedance to 50 ohm.



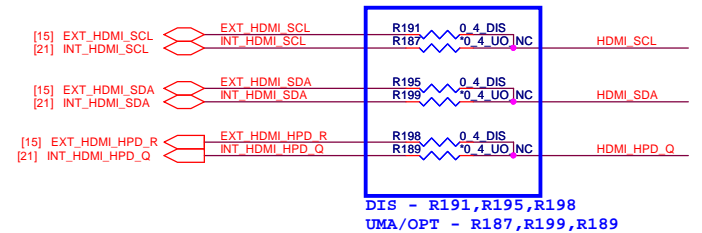
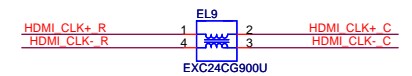
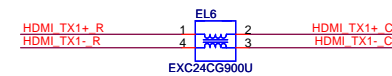
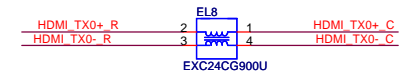
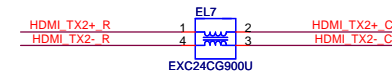
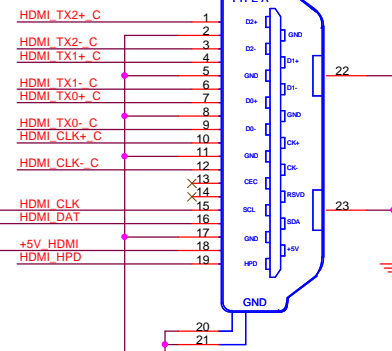
DIS HDMI



OTP/UMA HDMI

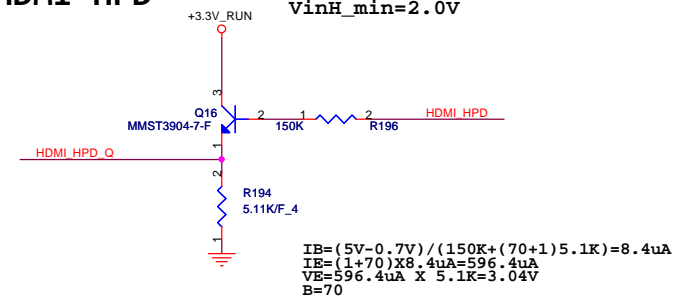


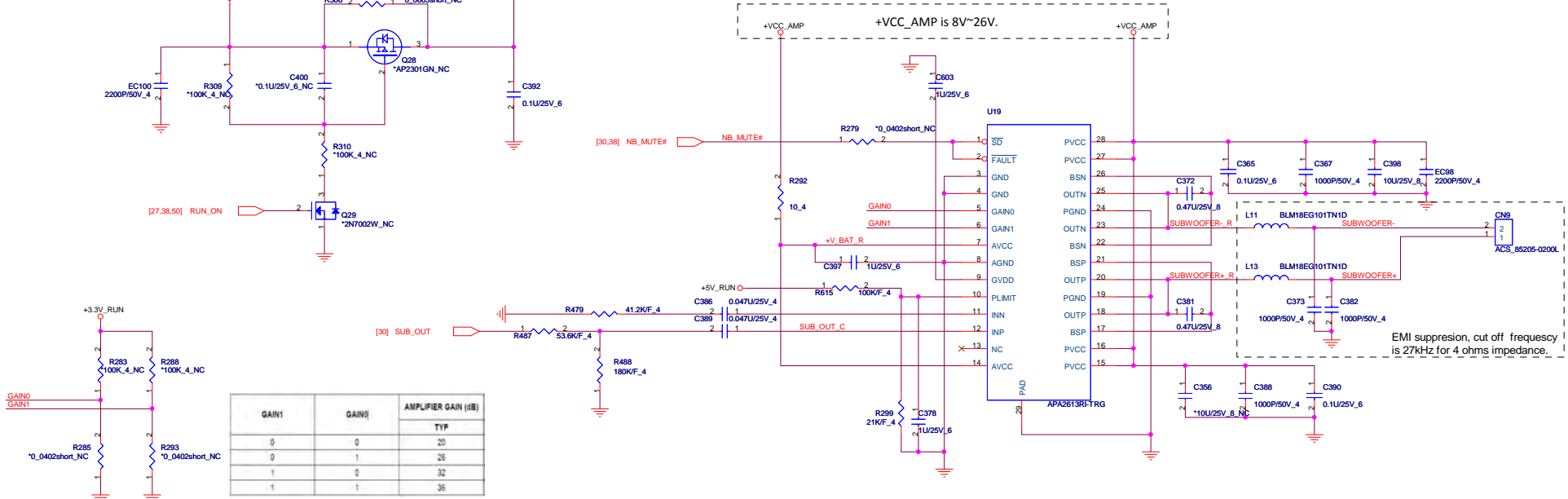
HDMI Conn.



HDMI HPD

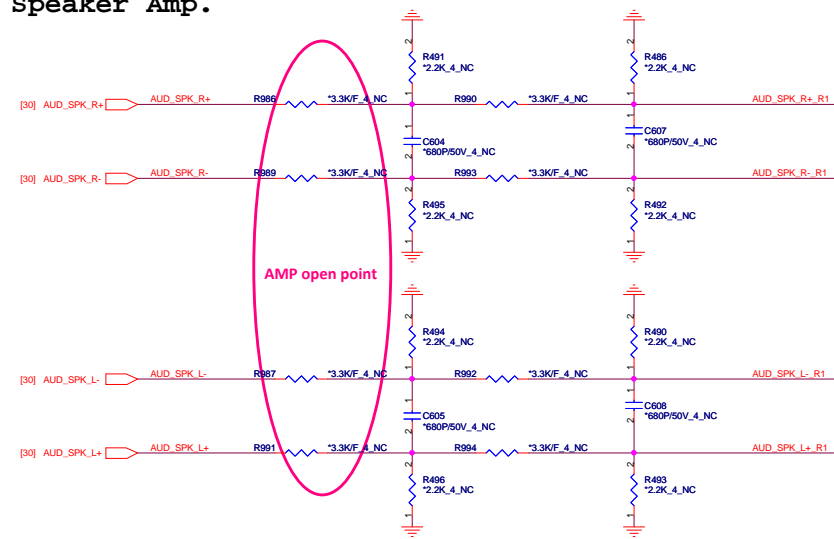
HDMI_HPD spec
VinH_min=2.0V



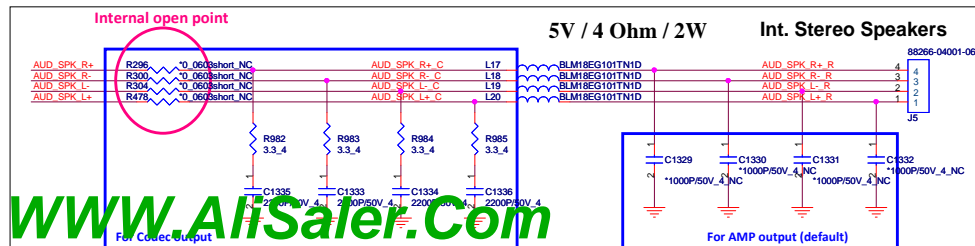
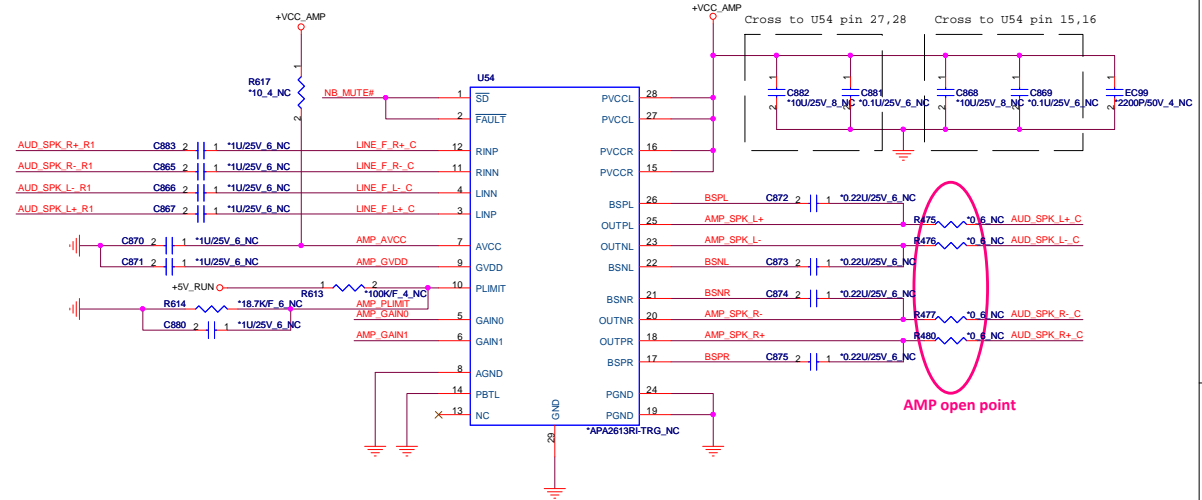


Speaker Amp.

R491,R495,R494,R496 default NC



APA2613 is P2P to TI TPA3113



A

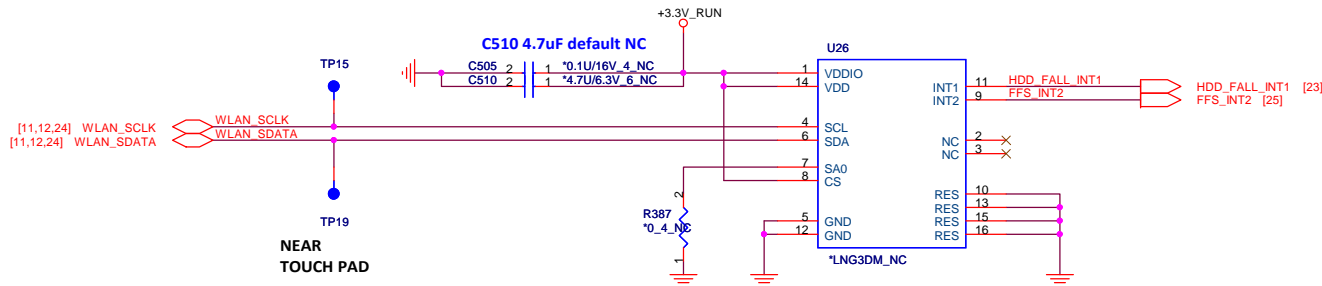
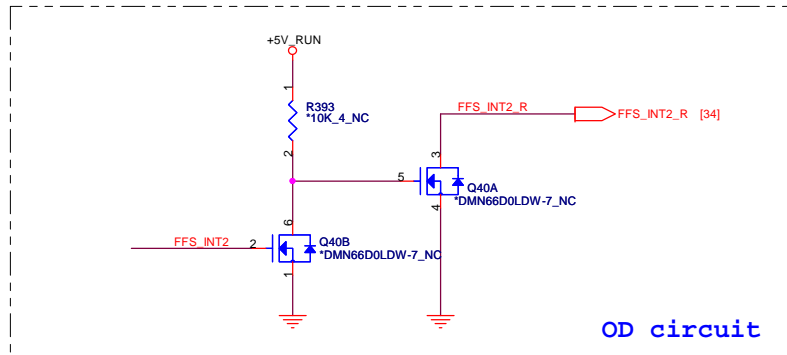


A

A

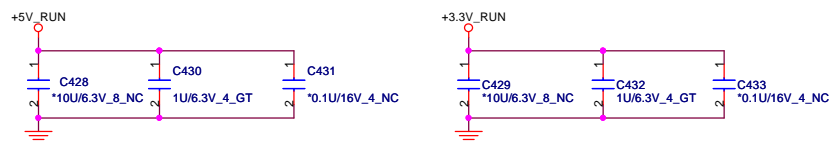
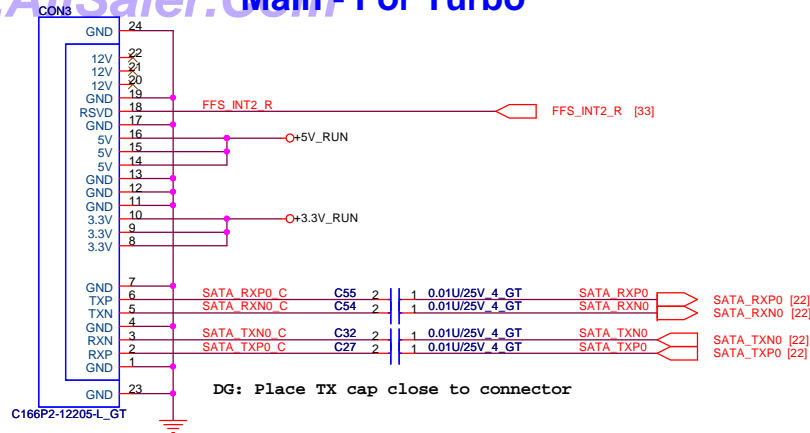
A

3-axis Fall Sensor - NC



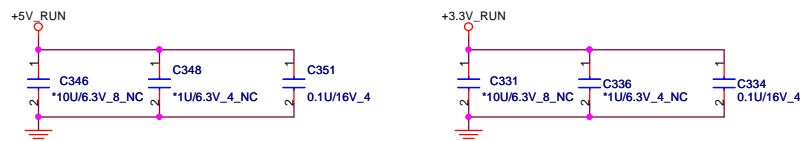
SA0 is low: I2C device address is 00110000 (30h)

SA0 is high: I2C device address is 00110010 (32h)

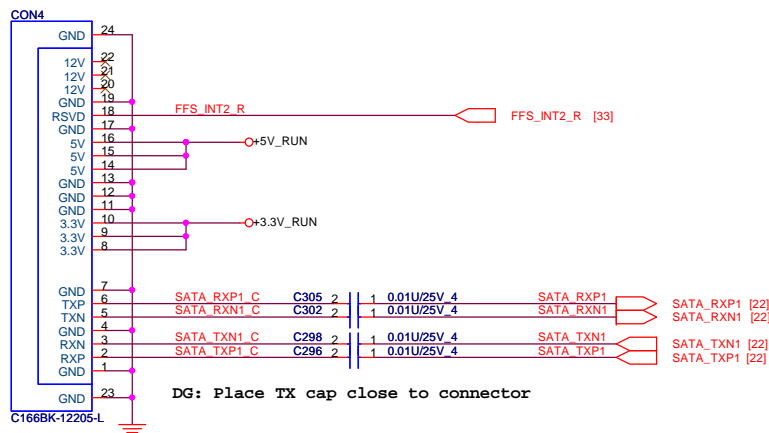


Default C351, C430 POP

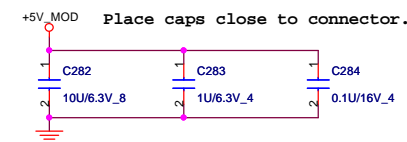
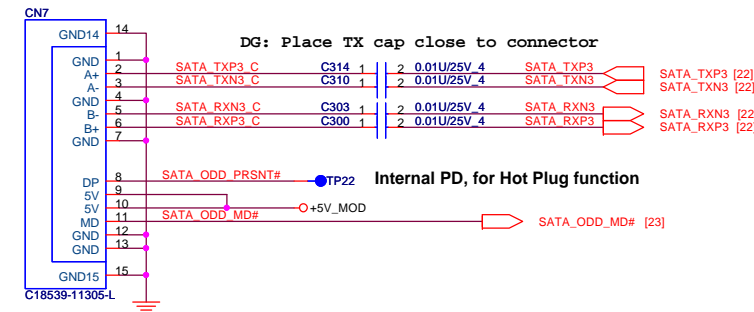
Default C334, C432 POP



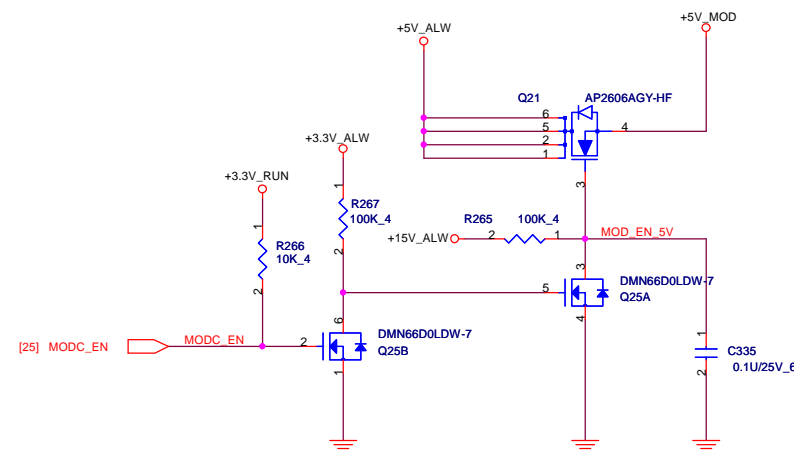
Second - For Inspiron



ODD

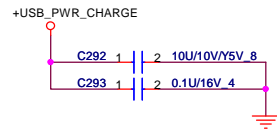
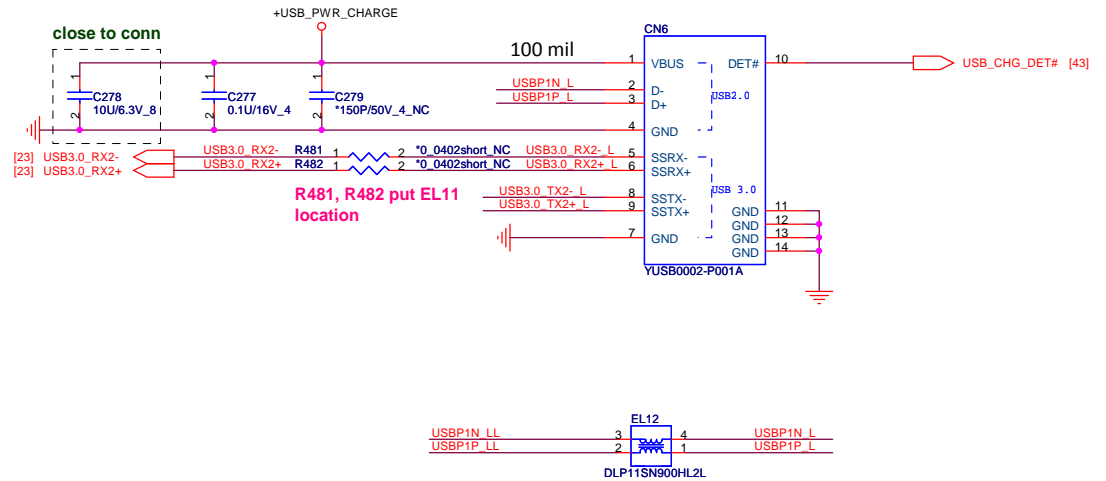
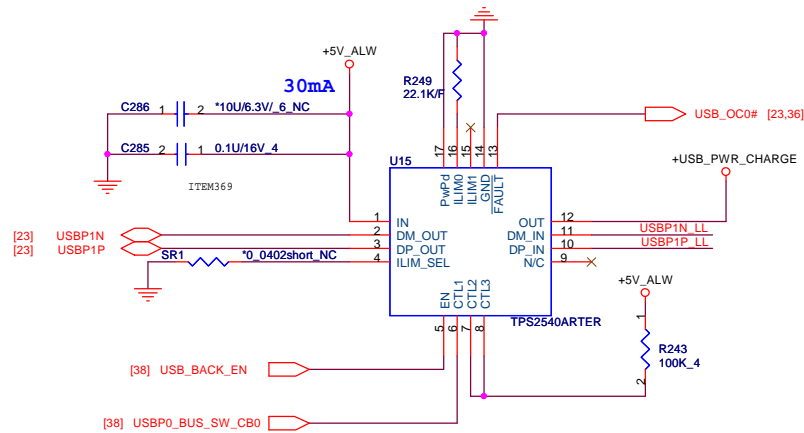


Support Zero power ODD



Quanta Computer Inc.
PROJECT : R09A

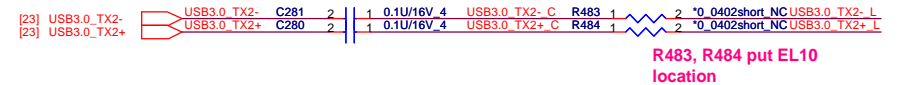
USB3.0x1 with Power share



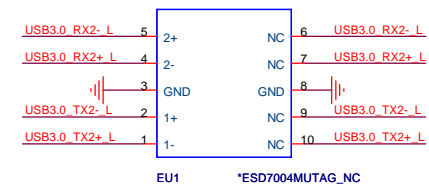
	R249	mA
OC limitation	100k ohm	480
	22.1k ohm	2171

Applied Now

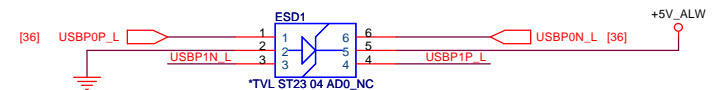
USBP0_BUS_SW_CB0	Mode	Operating at
Low	DCP, Auto-detect	S3/S4/S5, 1.5 A
High	CDP, BC Spec 1.1	S0, 1.5 A

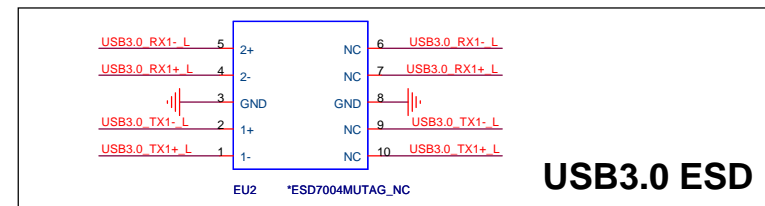
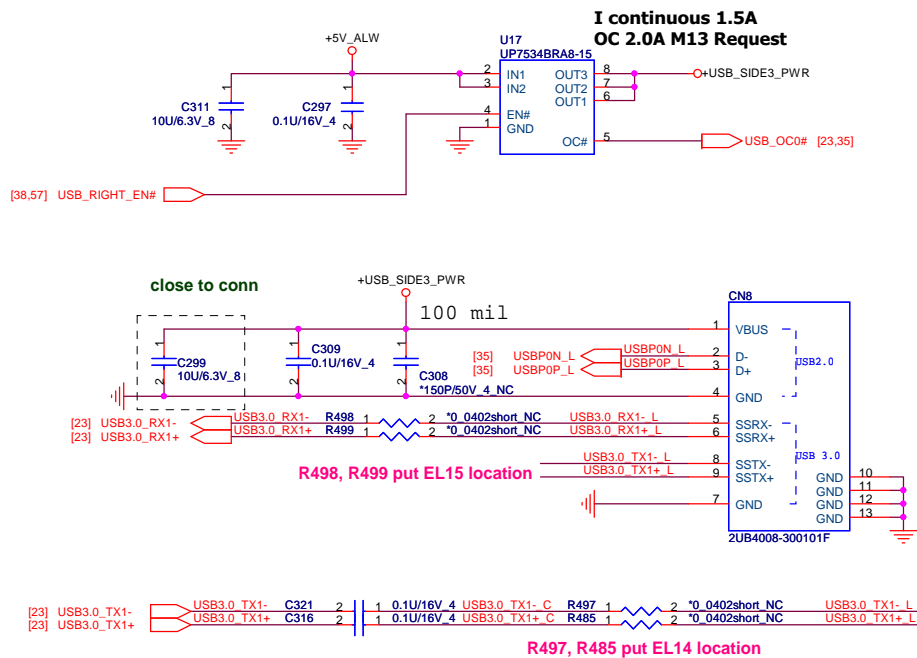


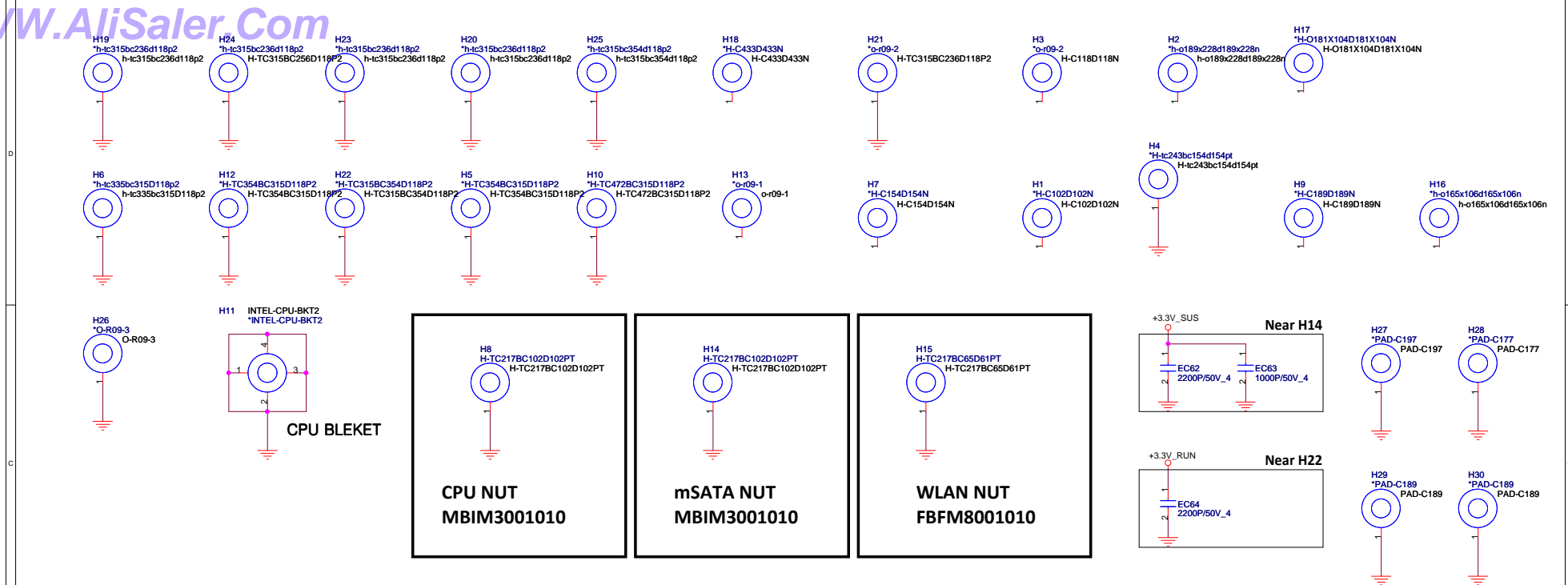
USB 3.0 ESD



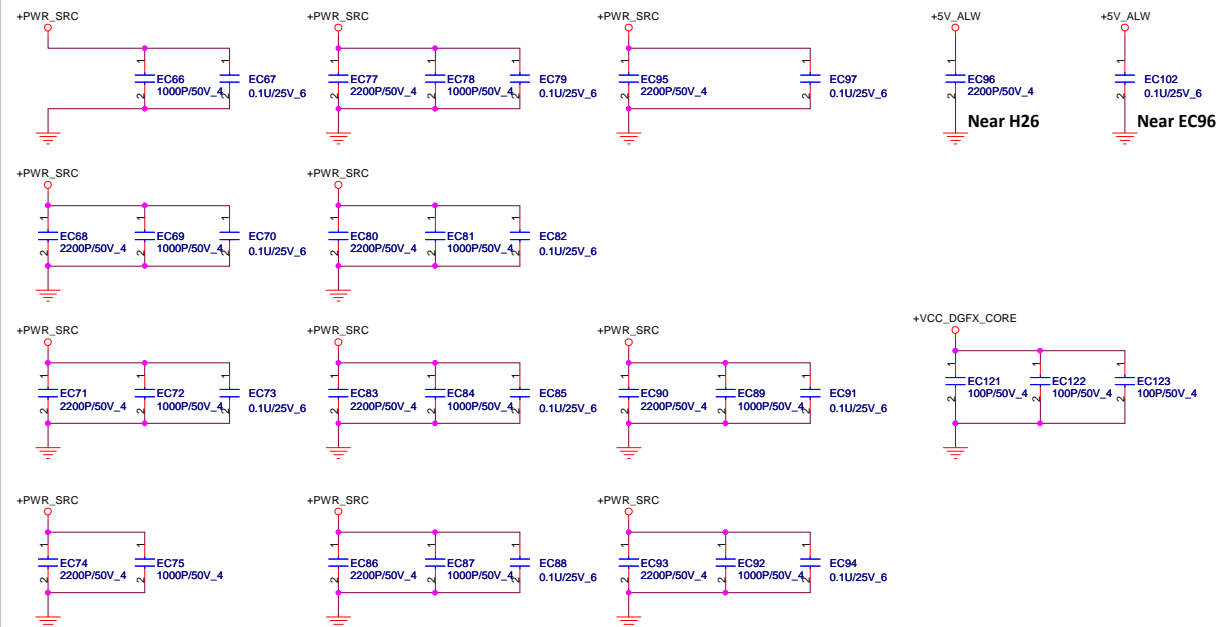
USB 2.0 ESD



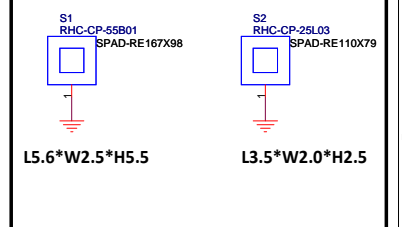




Near
C423/ESD2/H8/PR204/PR235/pq20/PL5/PC121/H10/R334/PL7/EC45



Spring



AOI label

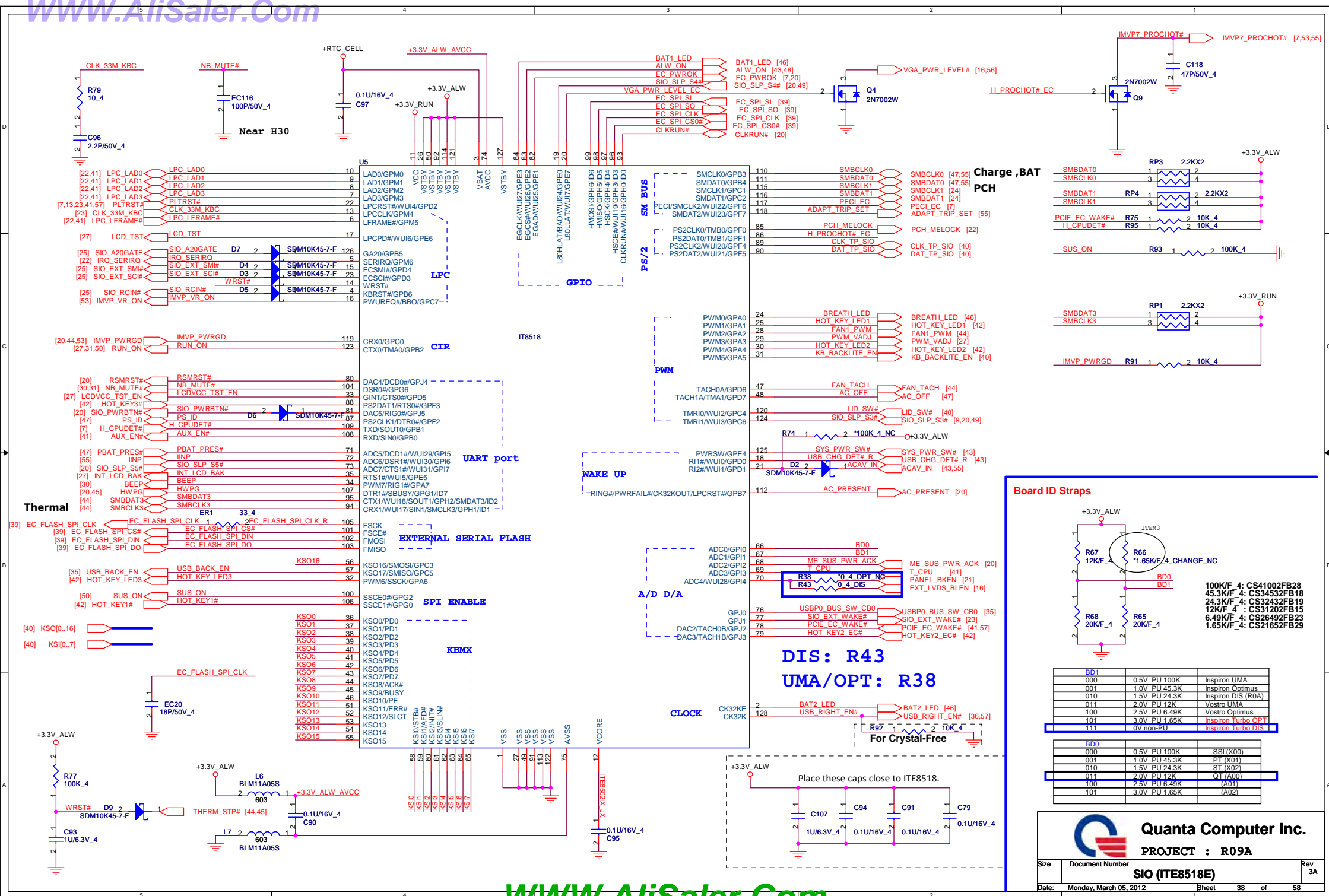
AOI LABEL on 31 header

PPID label

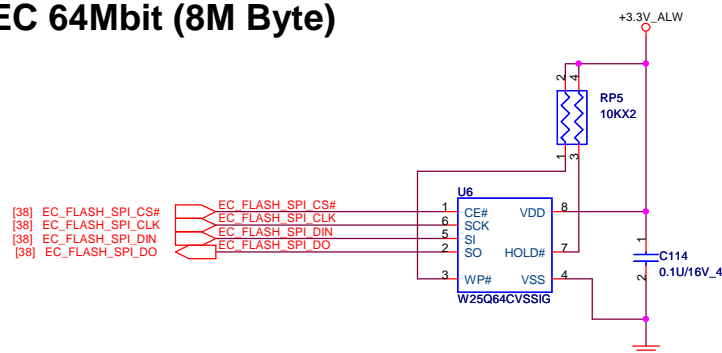
PPID LABEL on 31 header

AOI label

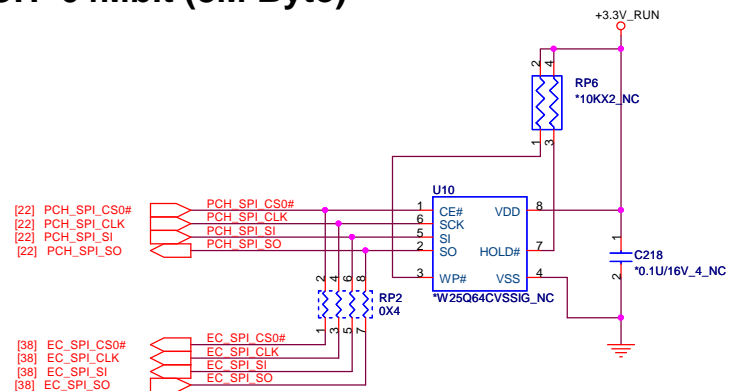
AOI LABEL on 31 header



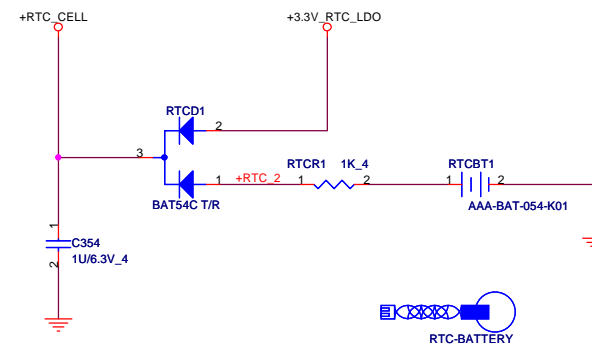
For EC 64Mbit (8M Byte)



For PCH 64Mbit (8M Byte)

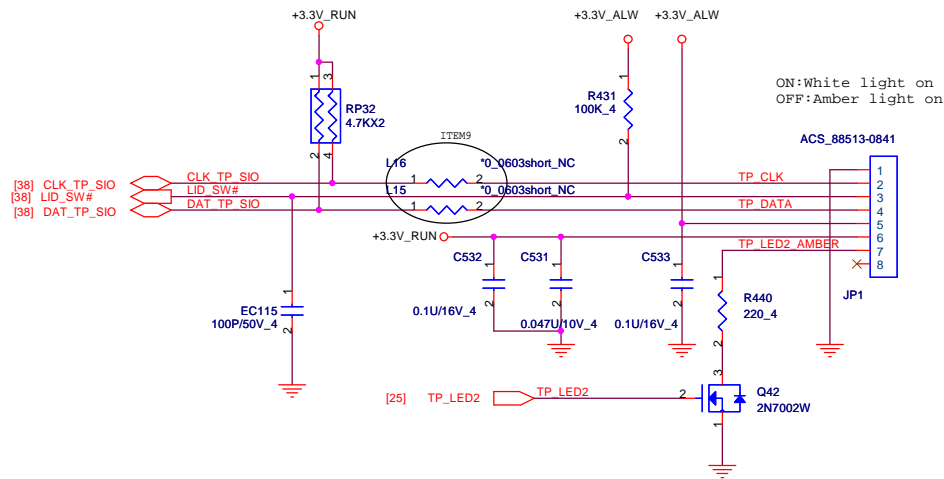


RTC

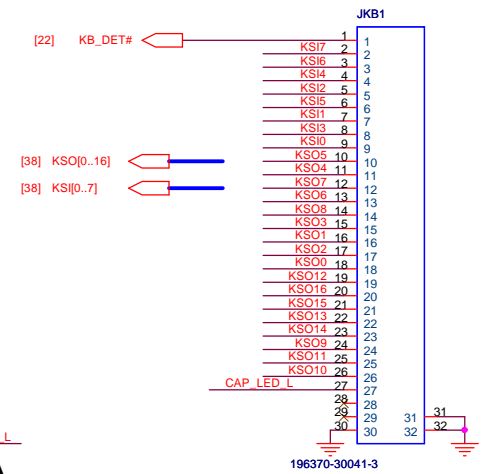
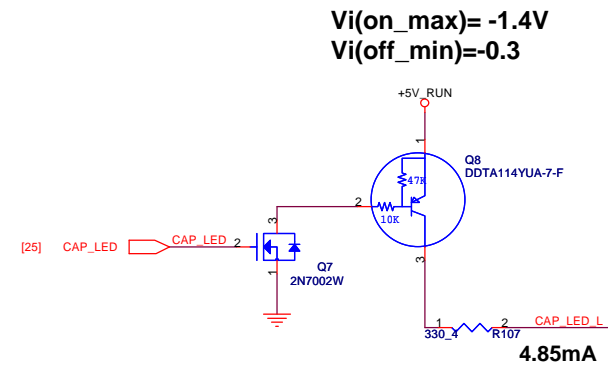


Double, 25°C, Vf=0.4V, If=25mA
one, 25°C, Vf=0.35V, If=15.8mA

Touch Pad CONNECTOR

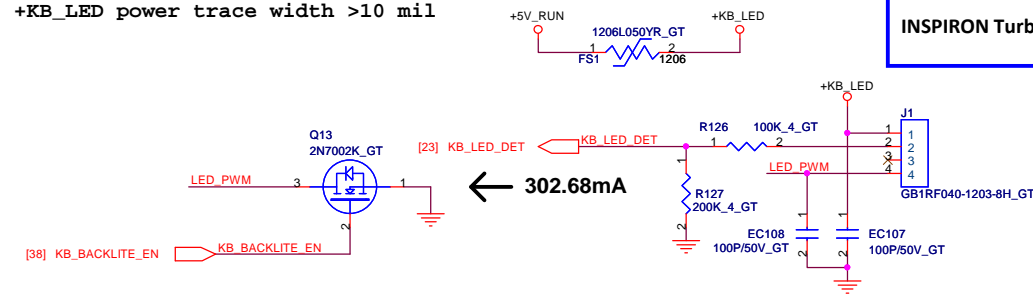


KEYBOARD CONNECTOR

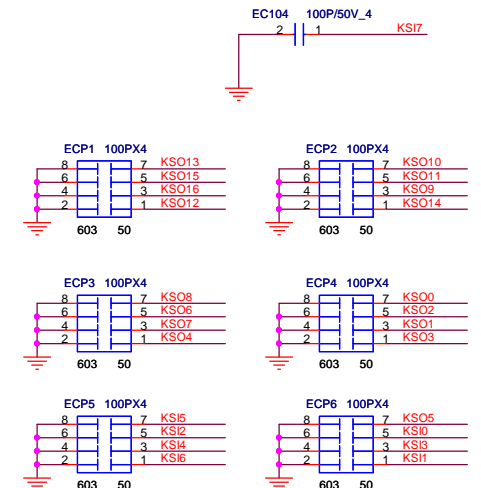


Key board illumination

+KB_LED power trace width >10 mil



INSPIRON	NC
INSPIRON Turbo	POP



Layout Note: 100P CAPS CLOSE TO JKB1

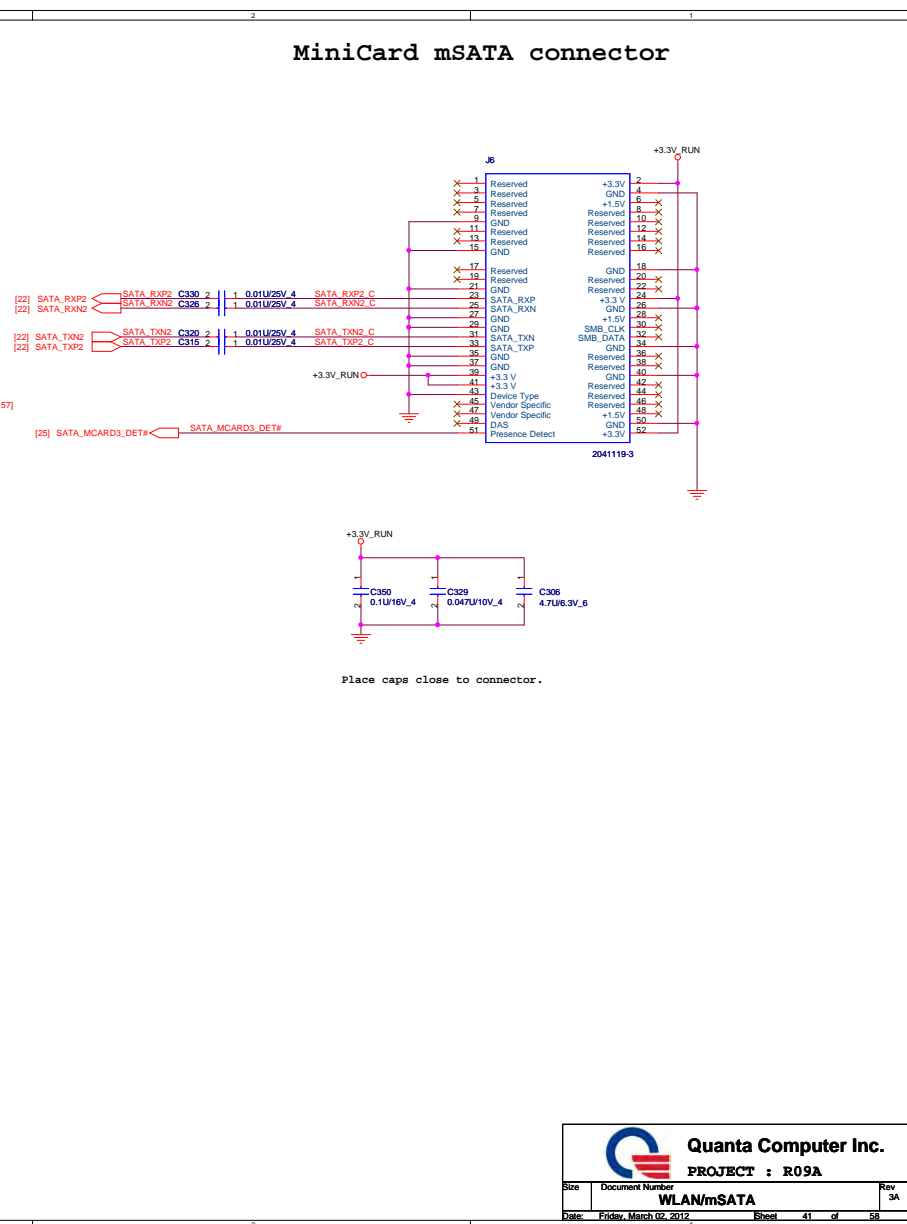


Quanta Computer Inc.

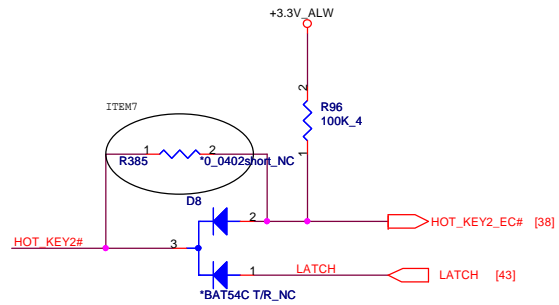
PROJECT : R09A

TP / KB

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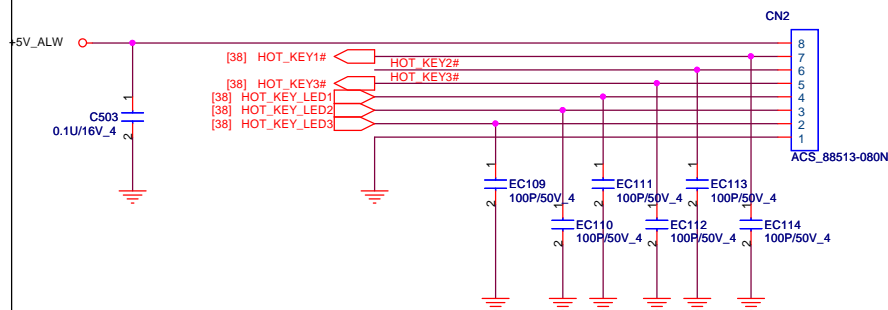


HOT_KEY2 support Pre-Boot Recovery

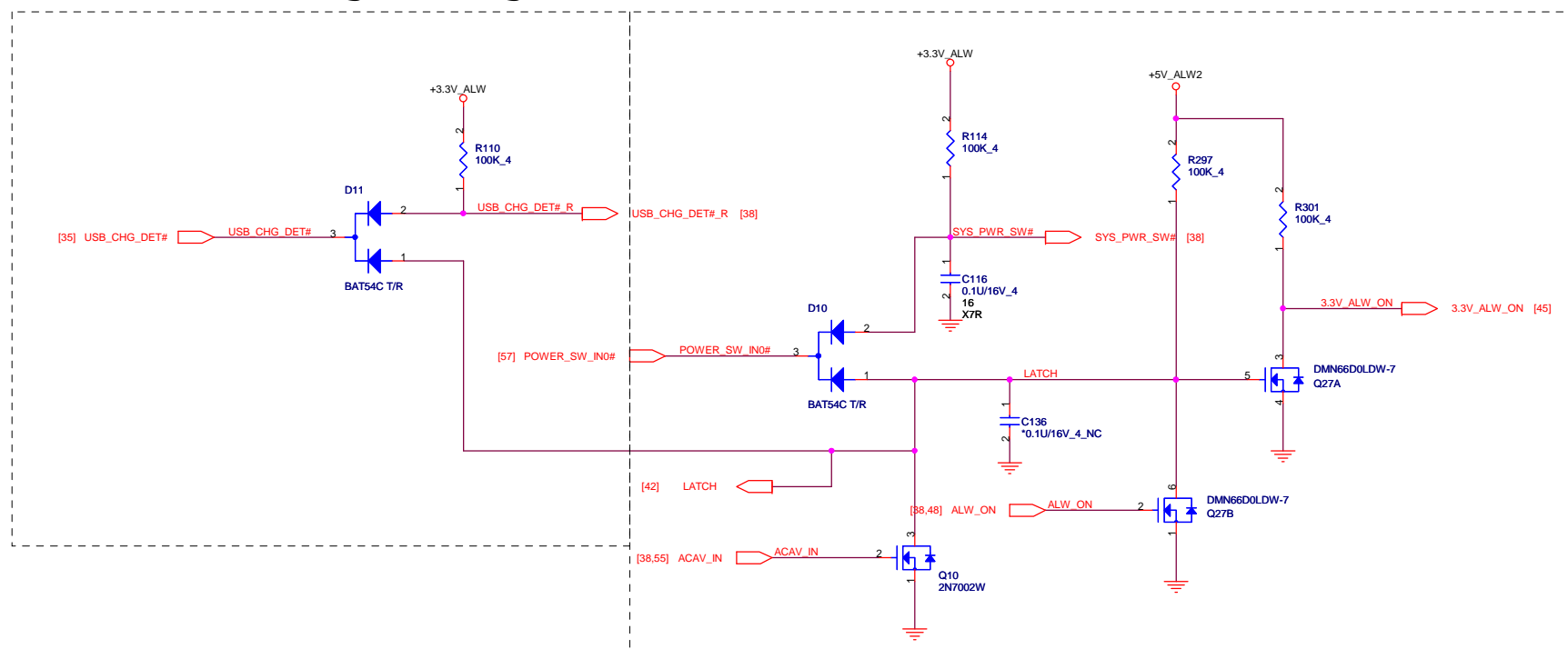


INSPIRON: R385 pop, D8 NC

Hot key BOARD



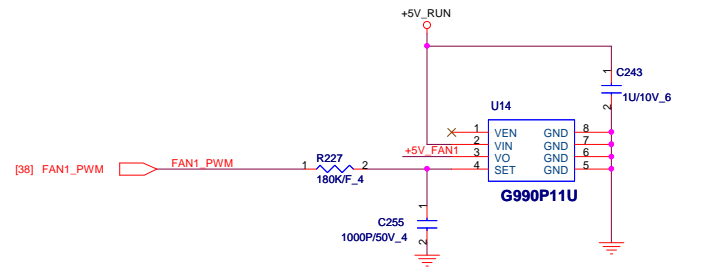
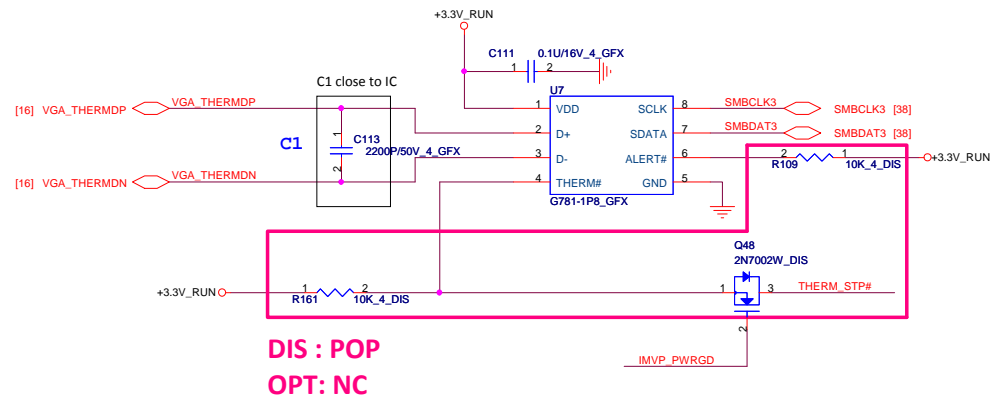
3V ALW ON POWER LOGIC



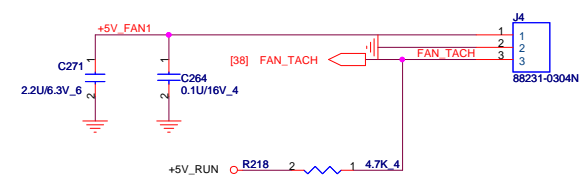
For GPU use

DIS/OPT:POP
UMA:NC

G781-1P8
SMBus address is 1001101xb (9Ah) (x is R/W bit).



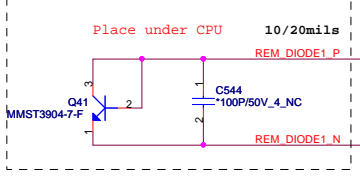
FAN CONN



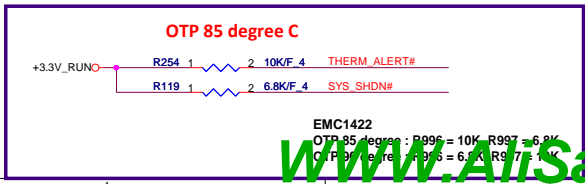
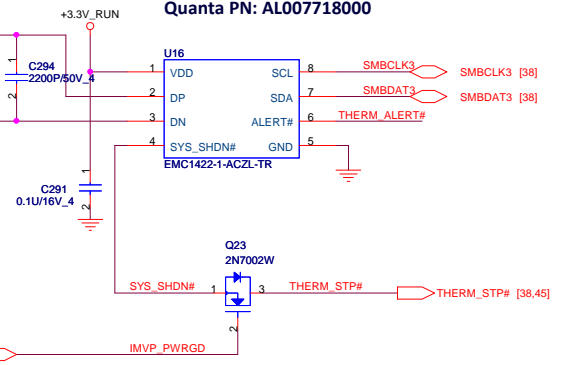
For CPU use

Low cost
EMC1422 pin to pin NCT7718W
NCT7718W
Quanta PN: AL007718000

Closed to CPU



- 1.Place C1340 close to NCT7718W
- 2.Place C1339 close to Q81
- Total capacitance between D+/D- is 2200pF(max)
- if use 2200pF for C1340, then C1339 should be dummy

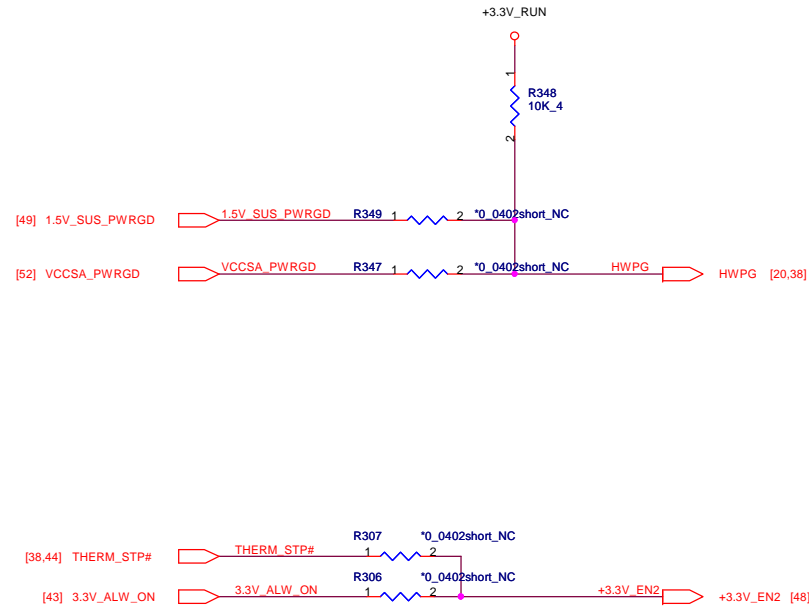


NCT7718W SMBus address is 1001100xb (98h) (x is R/W bit).

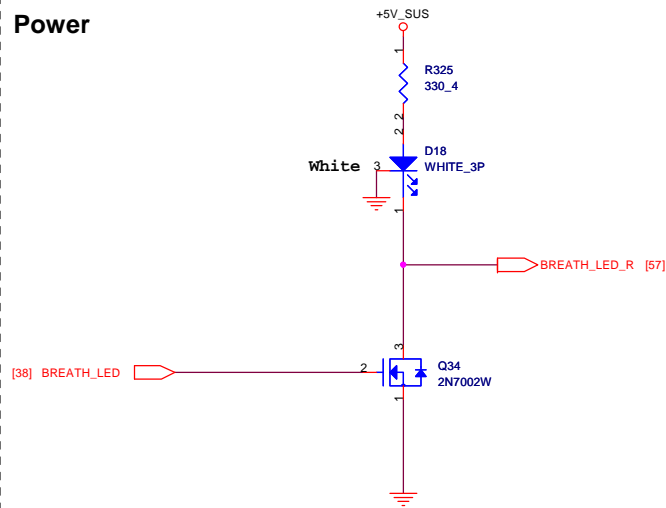
SYS_SHD#	2K	7.5K	10.5K	14K	18.7K
ALERT#	77'C	87'C	97'C	107'C	117'C
2K	77'C	87'C	97'C	107'C	117'C
7.5K	79'C	89'C	99'C	109'C	119'C
10.5K	81'C	91'C	101'C	111'C	121'C
14K	83'C	93'C	103'C	113'C	123'C
18.7K	85'C	95'C	105'C	115'C	125'C

EMC1422 SMBus address is 1001_100xb (98h) (x is R/W bit).

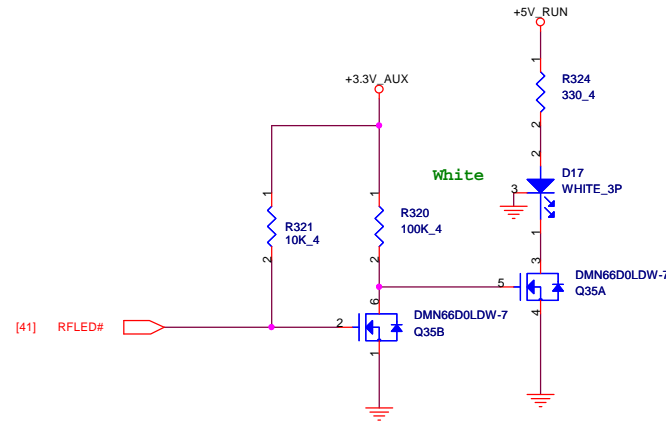
SYS_SHD#	4.7K	6.8K	10K	15K	22K	33K
ALERT#	77'C	83'C	89'C	95'C	101'C	107'C
4.7K	77'C	83'C	89'C	95'C	101'C	107'C
6.8K	78'C	84'C	90'C	96'C	102'C	108'C
10K	79'C	85'C	91'C	97'C	103'C	109'C
15K	80'C	86'C	92'C	98'C	104'C	110'C
22K	81'C	87'C	93'C	99'C	105'C	111'C
33K	82'C	88'C	94'C	100'C	106'C	112'C



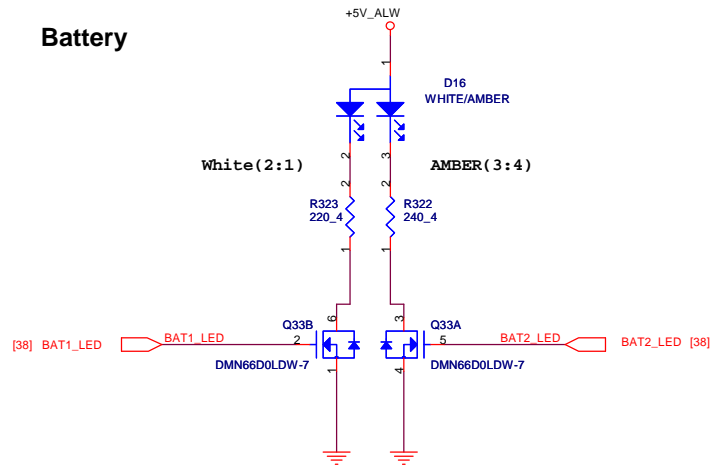
Power



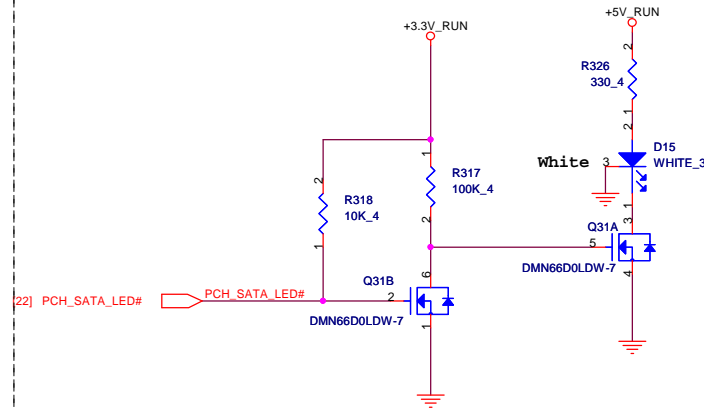
Bluetooth / WLAN on/off LED

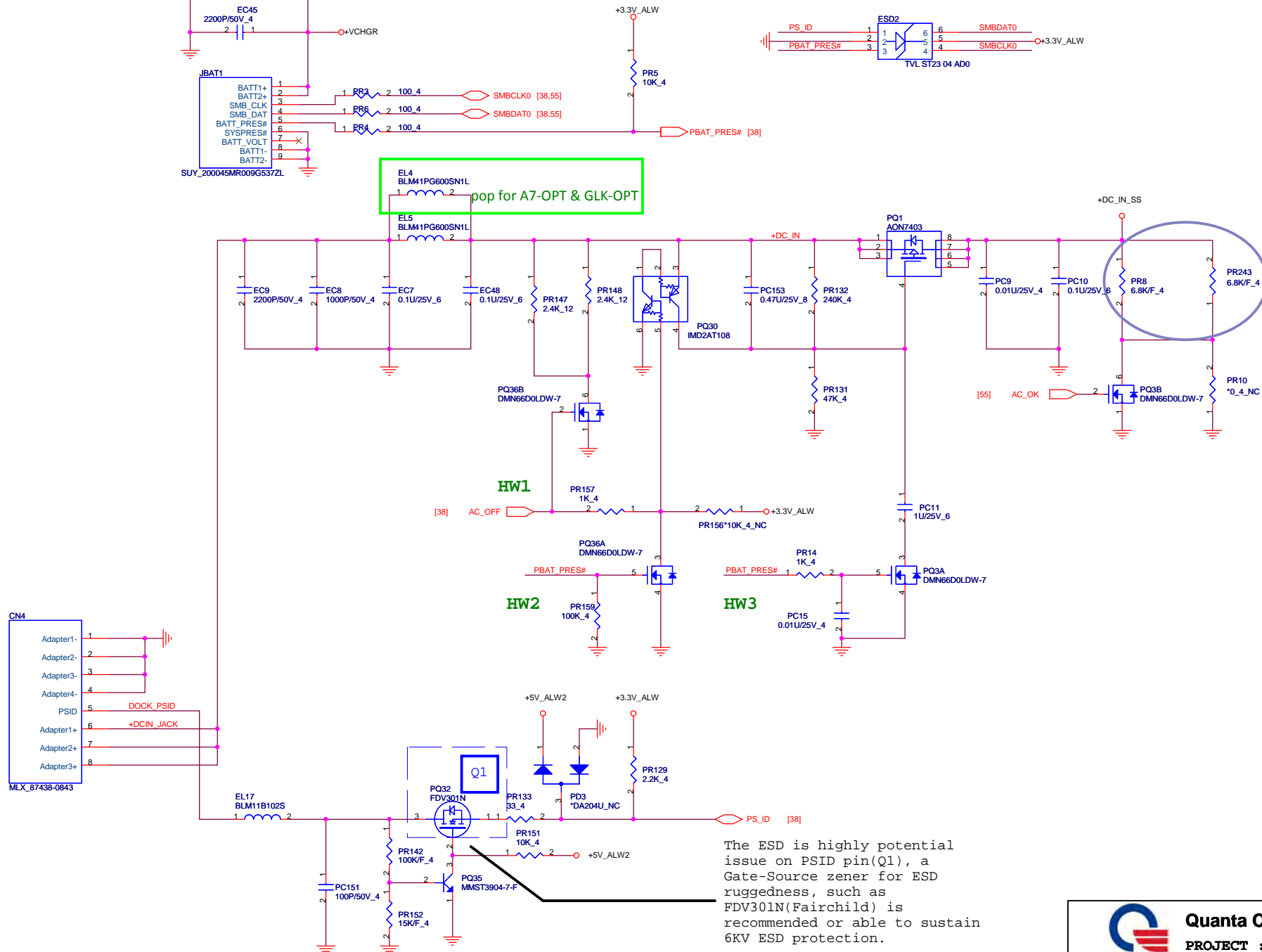



Battery

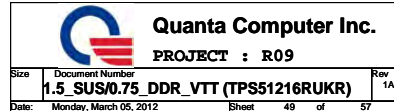


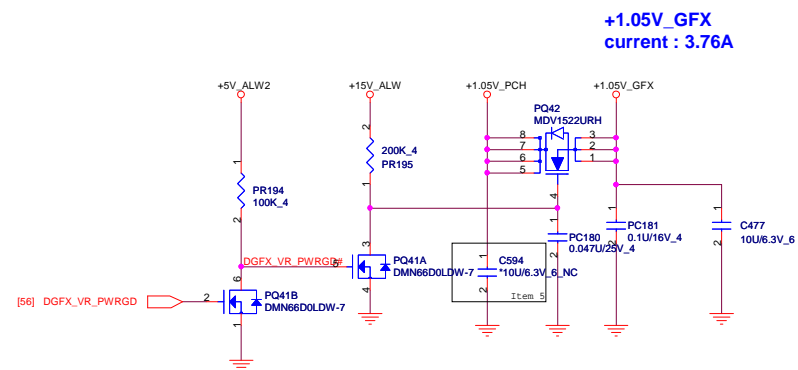
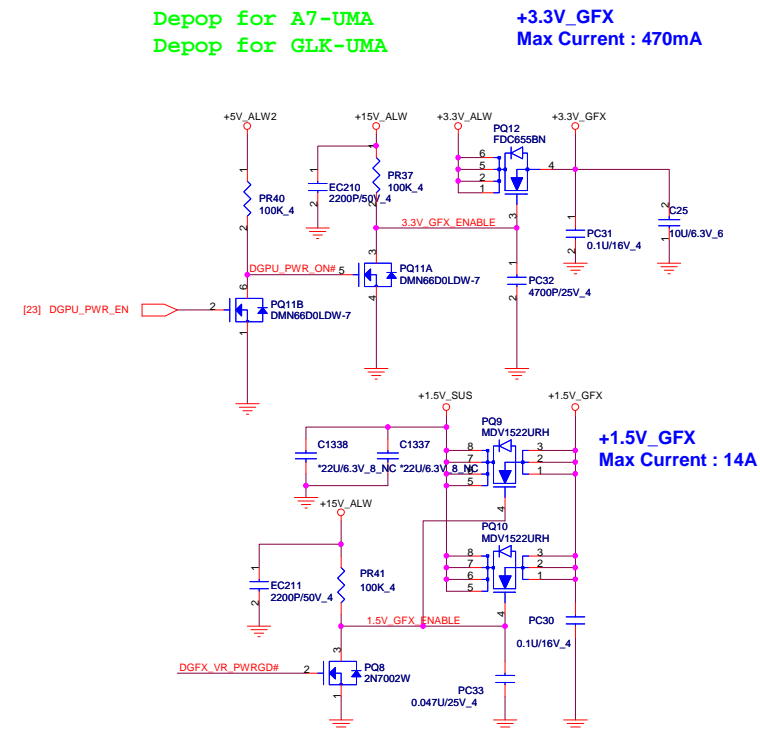
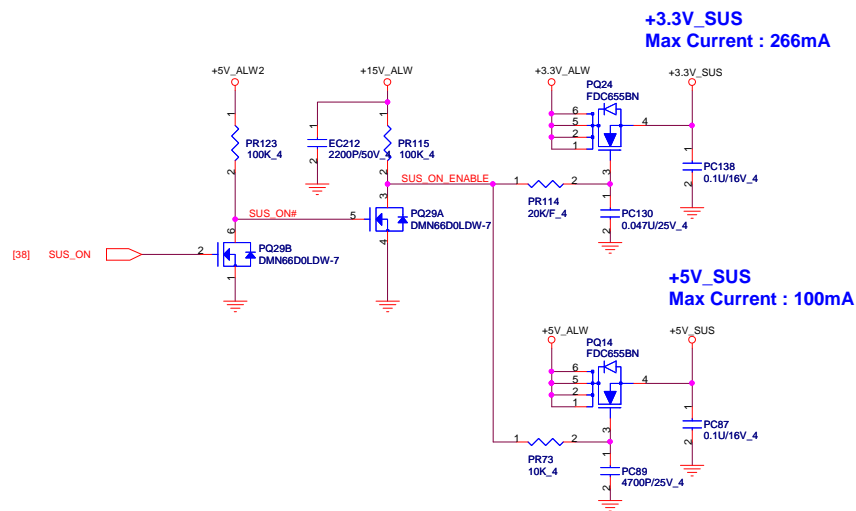
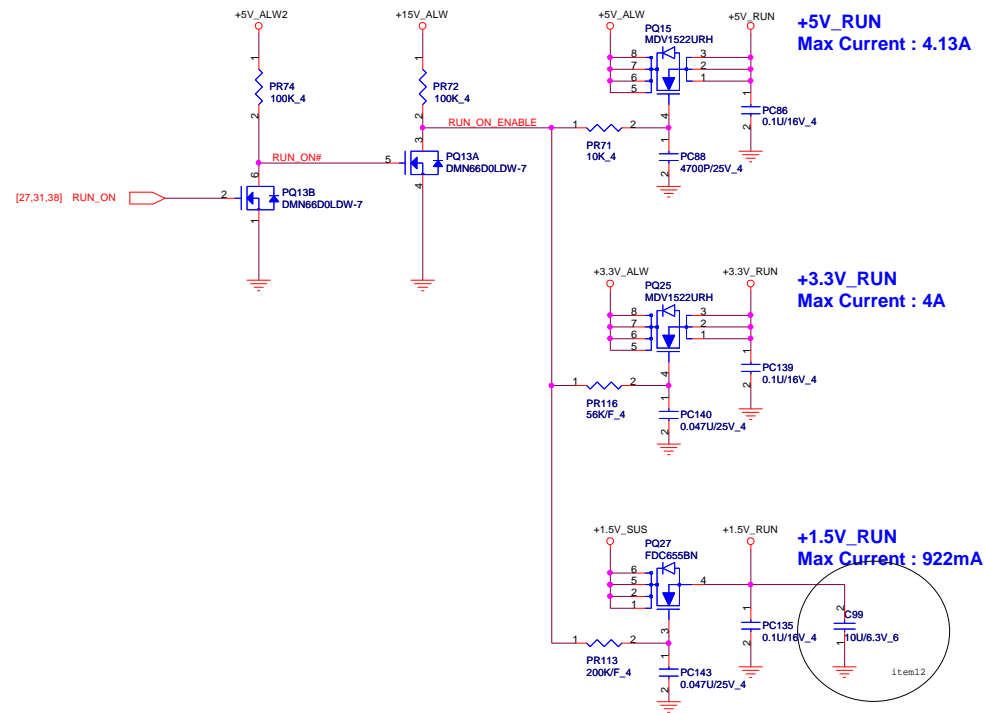
HDD activity LED.

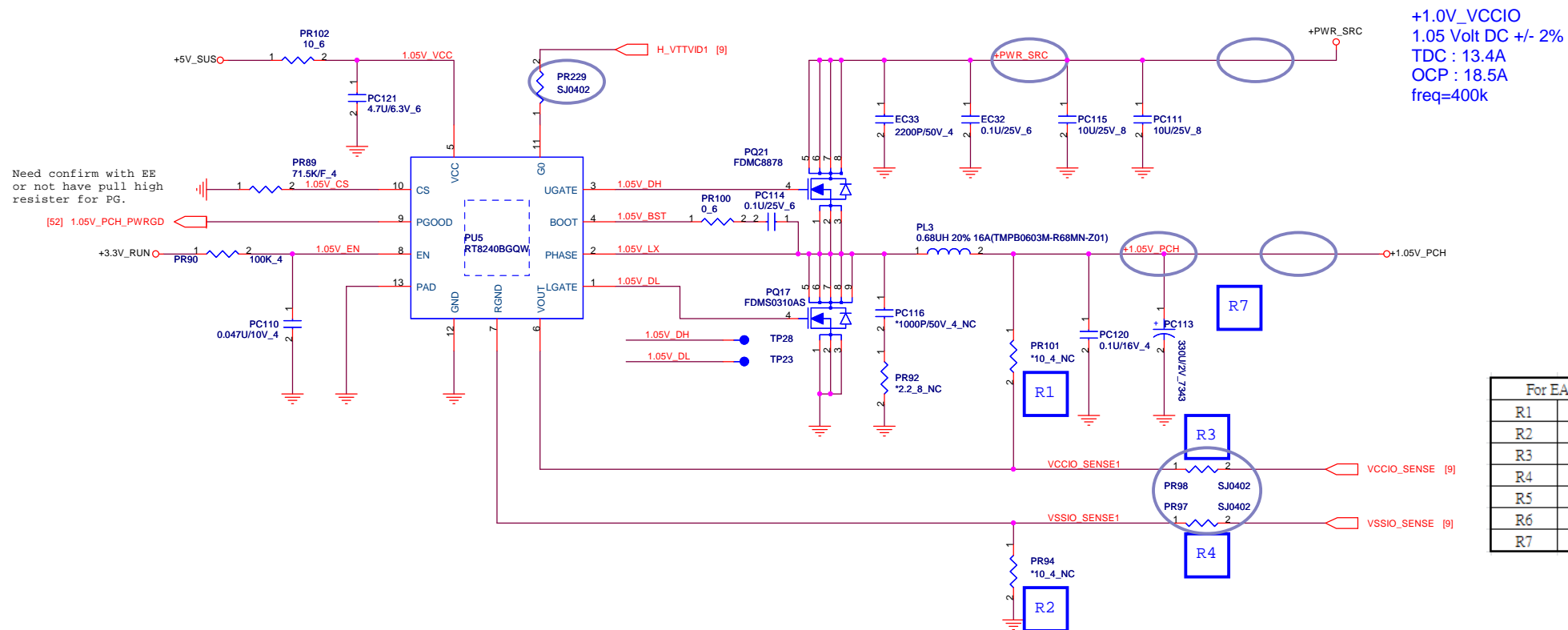


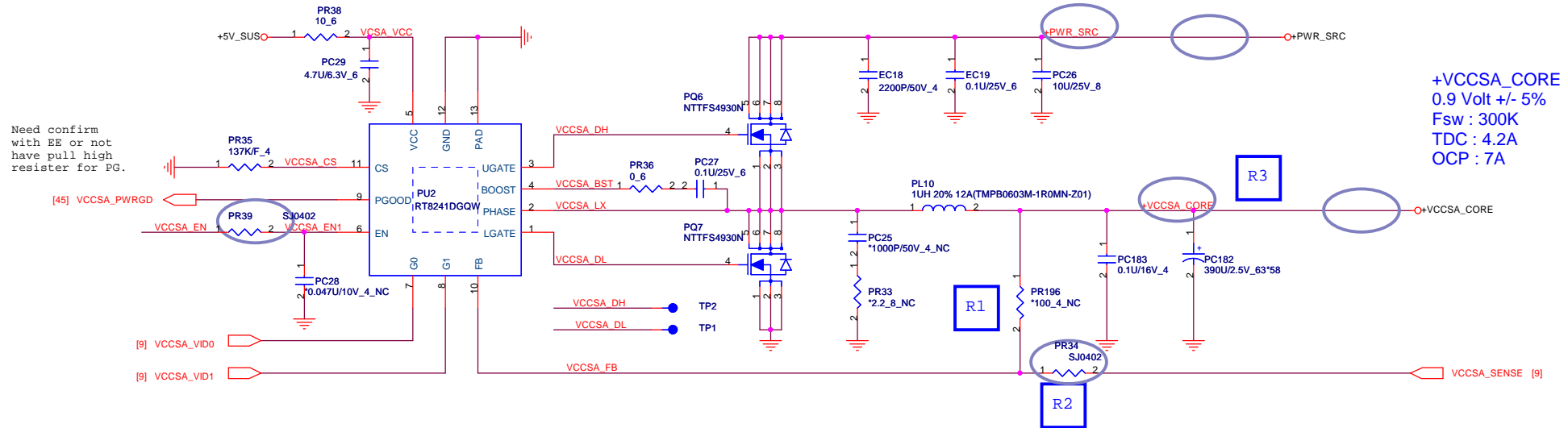


 Quanta Computer Inc. PROJECT : R09		
Size	Document Number 3.3V_ALW / 5V_ALW (TPS51125ARGER)	Rev 1A
Date:	Monday, March 05, 2012	Sheet 48 of 57



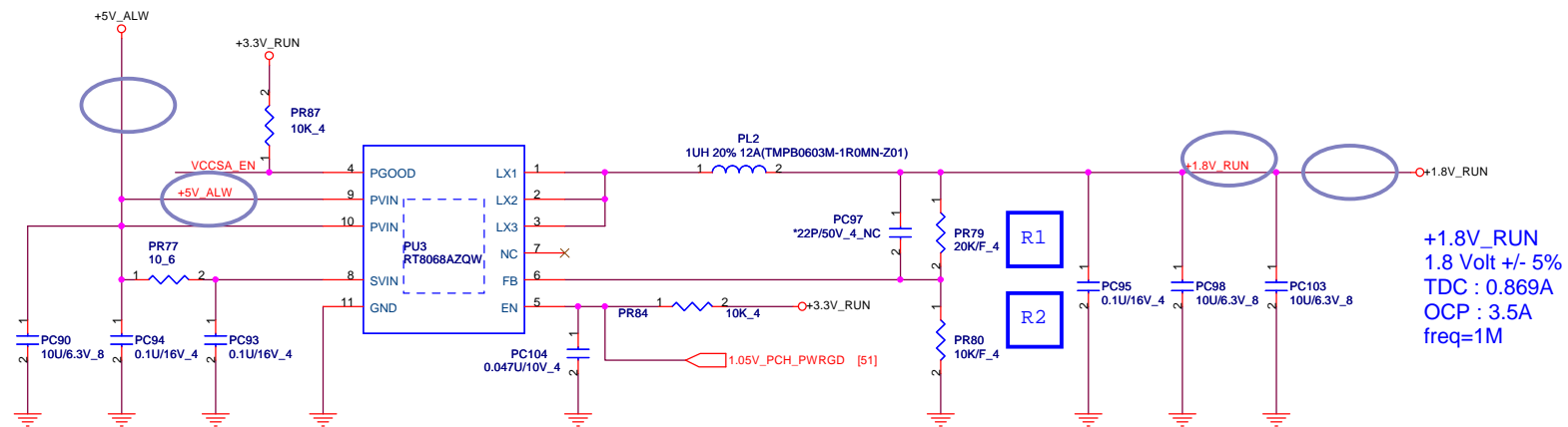






VCCSA_VID1	VCCSA_VID0	VCCSA_CORE
Low	Low	0.9V
High	Low	0.8V
Low	High	0.725V
High	High	0.675V

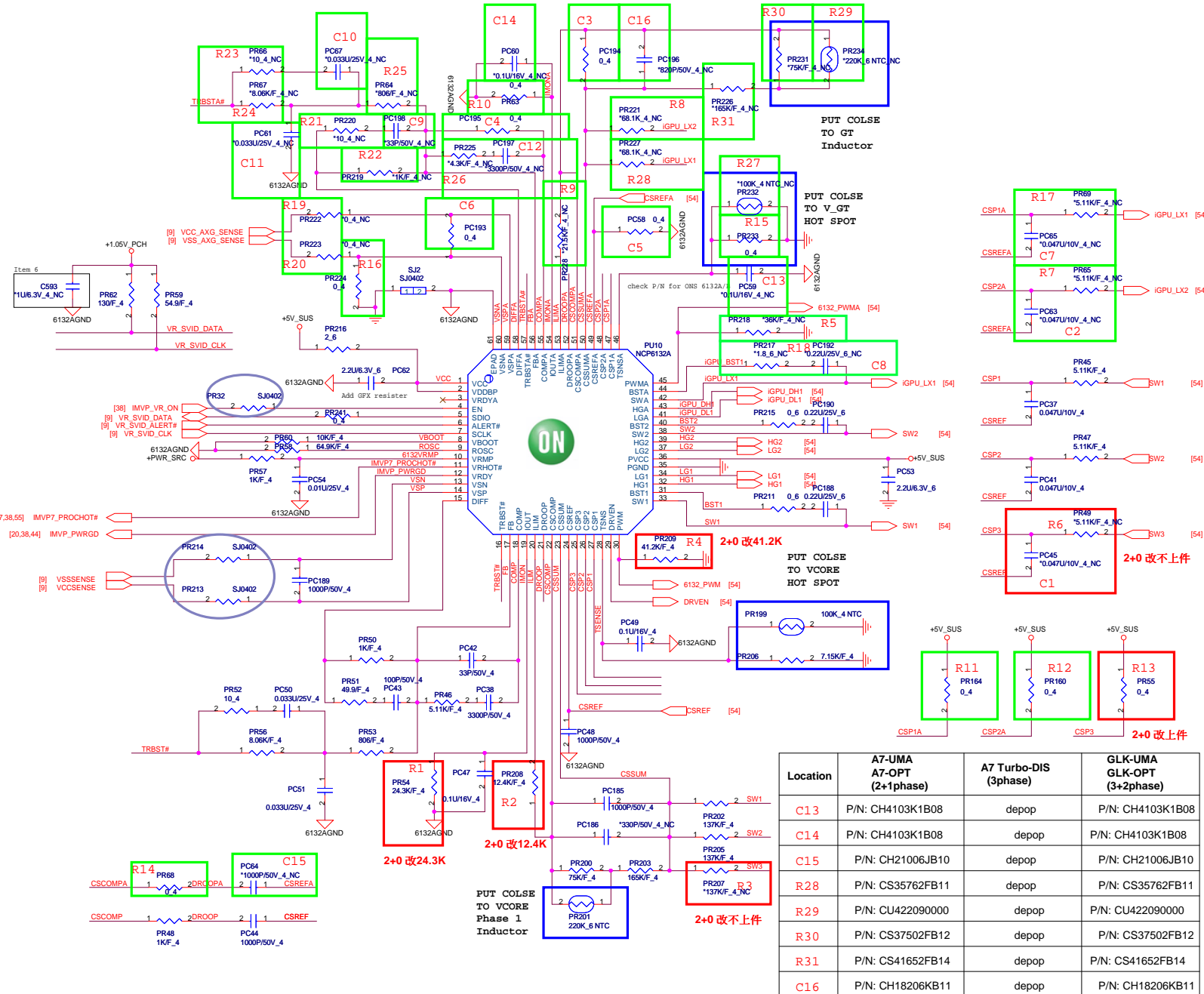
For EA test	
R1	100_4
R2	NC
R3	NC
R4	NC



$$VOUT = 0.6(1+R1/R2)$$



Quanta Computer Inc.
PROJECT : R09



Location	A7-UMA A7-OPT (2+1phase)	A7 Turbo-DIS (3phase)	GLK-UMA GLK-OPT (3+2phase)
R1	P/N: CS32432FB01	P/N: CS32372FB05	P/N: CS32372FB05
R2	P/N: CS31242FB05	P/N: CS32102FB14	P/N: CS32102FB14
R3	depop	P/N: CS41302FB01	P/N: CS41302FB01
R4	P/N: CS34122FB19	P/N: CS37322FB14	P/N: CS37322FB14
R5	P/N: CS32552FB03	depop	P/N: CS33602FB07
R6	depop	P/N: CS25112FB15	P/N: CS25112FB15
C1	depop	P/N: CH34702KB10	P/N: CH34702KB10
R7	depop	depop	P/N: CS25112FB15
C2	depop	depop	P/N: CH34702KB10
R8	depop	depop	P/N: CS35762FB11
R9	P/N: CS31582FB12	depop	P/N: CS32152B00
R10	P/N: CS32432FB01	P/N: CS00002JB38	P/N: CS32402FB15
R11	depop	P/N: CS00002JB38	depop
R12	P/N: CS00002JB38	P/N: CS00002JB38	depop
R13	P/N: CS00002JB38	depop	depop
C3	P/N: CH21006JB10	P/N: CS00002JB38	P/N: CH21006JB10
C4	P/N: CH01006JB08	P/N: CS00002JB38	P/N: CH01006JB08
C5	P/N: CH21006JB10	P/N: CS00002JB38	P/N: CH21006JB10
R14	P/N: CS15102FB19	P/N: CS00002JB38	P/N: CS15102FB19
C6	P/N: CH21006JB10	P/N: CS00002JB38	P/N: CH21006JB10
R15	P/N: CS28252FB15	P/N: CS00002JB38	P/N: CS28252FB15
R16	depop	P/N: CS00002JB38	depop
R17	P/N: CS25112FB15	depop	P/N: CS25112FB15
C7	P/N: CH34702KB10	depop	P/N: CH34702KB10
R18	P/N: CS00003J951	depop	P/N: CS00003J951
C8	P/N: CH4224K9904	depop	P/N: CH4224K9904
R19	P/N: CS00002JB38	depop	P/N: CS00002JB38
R20	P/N: CS00002JB38	depop	P/N: CS00002JB38
R21	P/N: CS01002JB22	depop	P/N: CS01002JB22
R22	P/N: CS21002FB24	depop	P/N: CS21002FB24
C9	P/N: CH03306JB04	depop	P/N: CH03306JB04
R23	P/N: CS01002JB22	depop	P/N: CS01002JB22
R24	P/N: CS22002FB19	depop	P/N: CS22002FB19
C10	P/N: CH16806KB17	depop	P/N: CH16806KB17
C11	P/N: CH24704KB19	depop	P/N: CH24704KB19
R25	P/N: CS31072FB10	depop	P/N: CS31072FB10
R26	P/N: CS24302FB07	depop	P/N: CS24302FB07
C12	P/N: CH23306JB16	depop	P/N: CH23306JB16
R27	P/N: CU4100B0000	depop	P/N: CU4100B0000

Location	A7-UMA A7-OPT (2+1phase)	A7 Turbo-DIS (3phase)	GLK-UMA GLK-OPT (3+2phase)
C13	P/N: CH4103K1B08	depop	P/N: CH4103K1B08
C14	P/N: CH4103K1B08	depop	P/N: CH4103K1B08
C15	P/N: CH21006JB10	depop	P/N: CH21006JB10
R28	P/N: CS35762FB11	depop	P/N: CS35762FB11
R29	P/N: CU422090000	depop	P/N: CU422090000
R30	P/N: CS37502FB12	depop	P/N: CS37502FB12
R31	P/N: CS41652FB14	depop	P/N: CS41652FB14
C16	P/N: CH18206KB11	depop	P/N: CH18206KB11

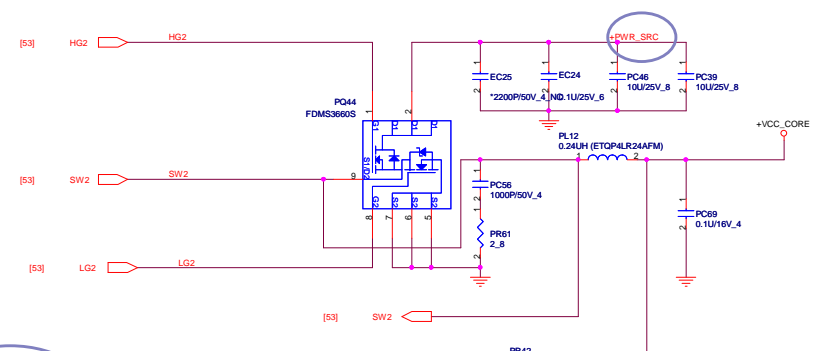
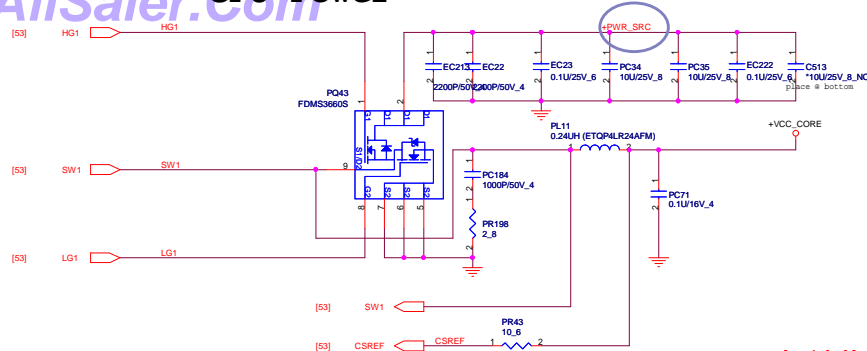


Quanta Computer Inc.

PROJECT : R09

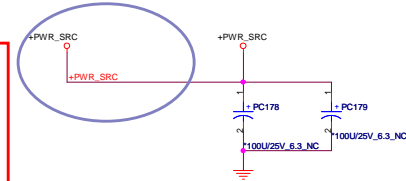
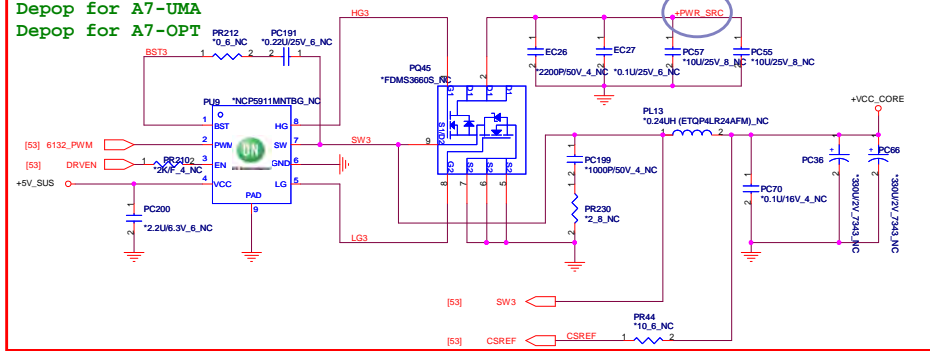
Size Document Number CPU CORE (NCP6132) Rev 1A

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2+0 改不上件

Depop for A7-UMA
Depop for A7-OPT

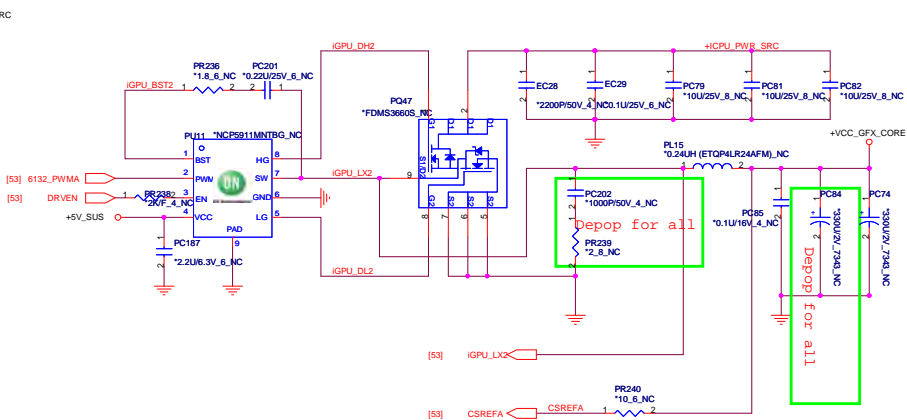
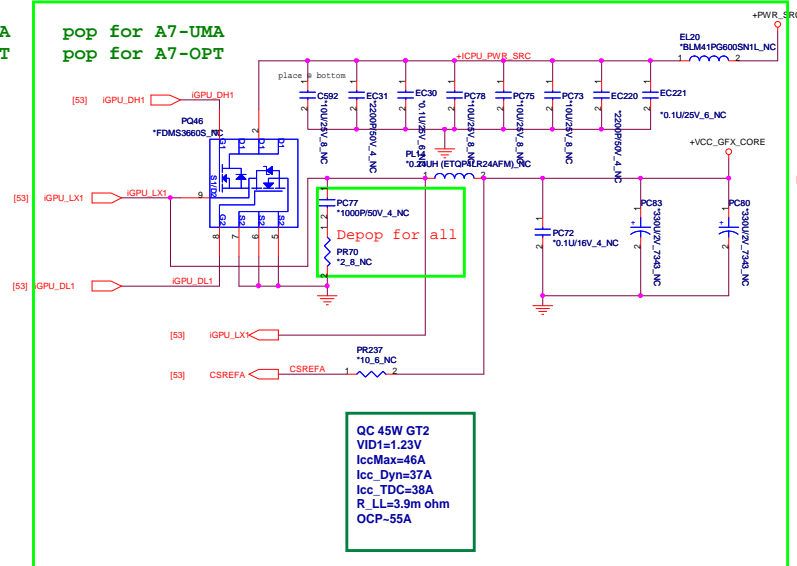


QC 45W CPU
VID1=0.9V
IccMax=94A
IccDyn=66A
IccTDC=52A
R_LL=1.9m ohm
OCP=110A

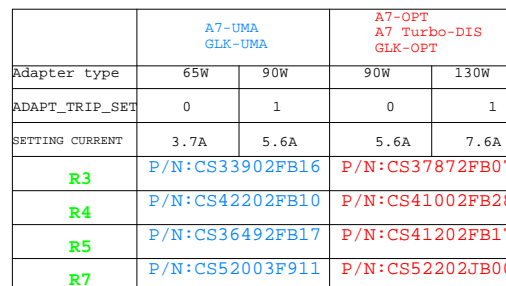


pop for GLK UMA
pop for GLK OPT

pop for A7-UMA
pop for A7-OPT



QC 45W GT2
VID1=1.23V
IccMax=46A
IccDyn=37A
IccTDC=38A
R_LL=3.9m ohm
OCP=55A



Depop for A7-UMA
Depop for GLK-UMA

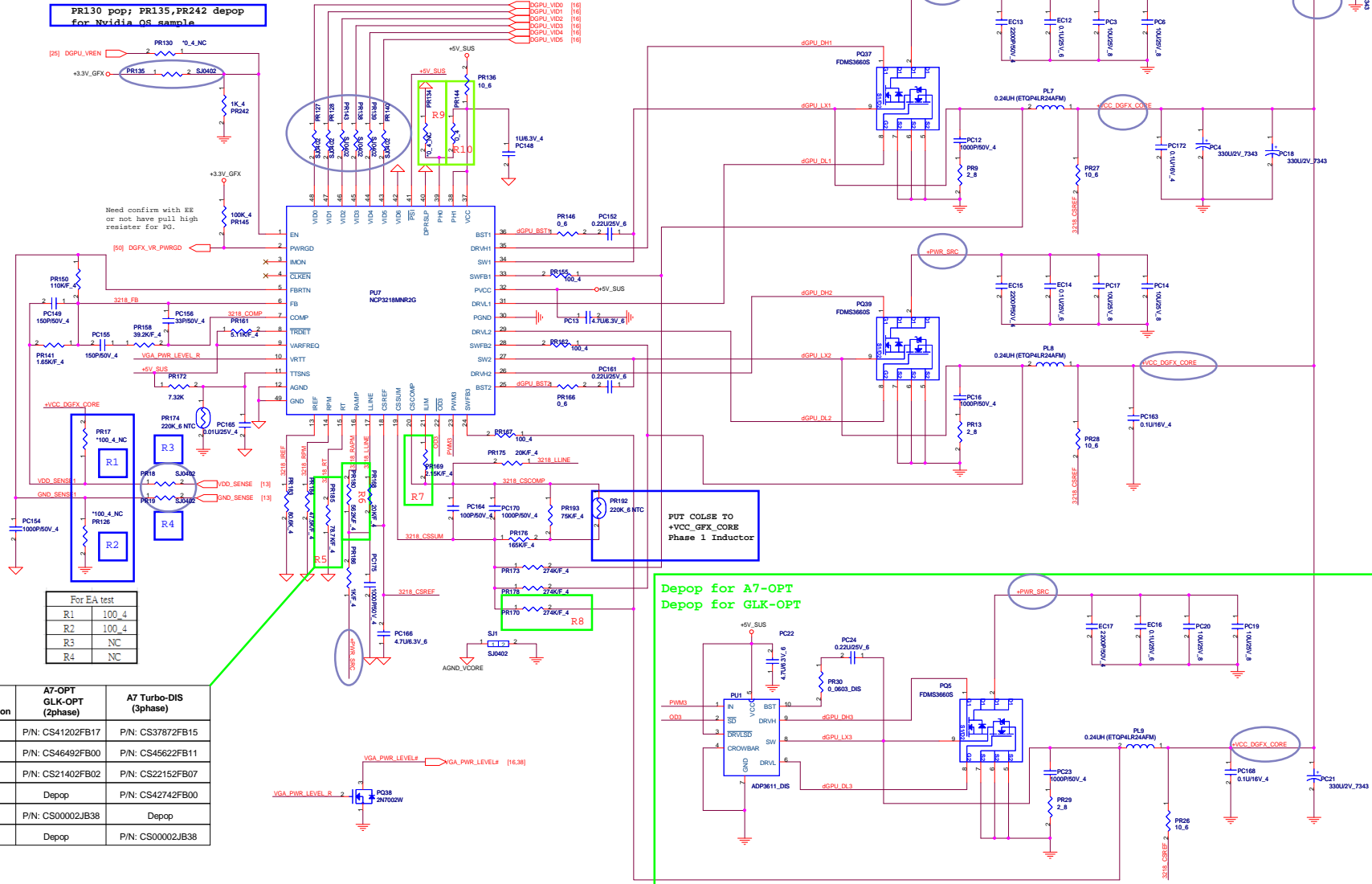
N13XXX2

	DGPU_VID3	DGPU_VID2	DGPU_VID1
0.85V	1	0	1
0.95V	0	1	1
1.0V	0	1	0

N13XXX1

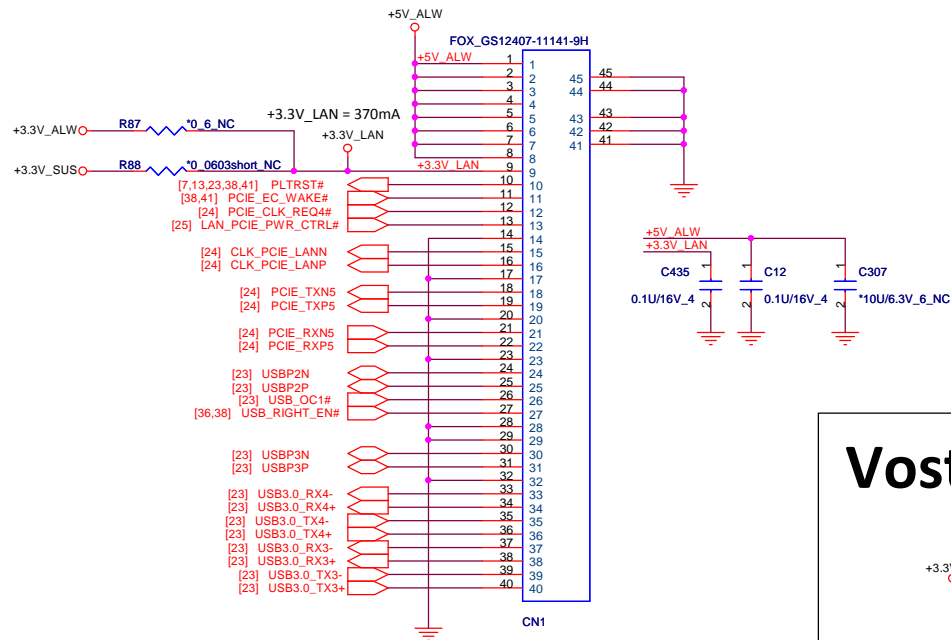
	DGPU_VID3	DGPU_VID2	DGPU_VID1
0.825V	1	0	1
0.975V	0	1	0
1.0V	0	0	1

+VCC_GFX_CORE
F_s=400K
Dis=30A
Turbo=42A
Dis OC=42A
Turbo OC=60A



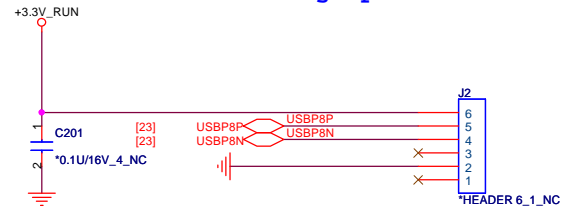
DB CONNECTOR

RJ45 + USB 3.0* 2



Vostro - NA

Fingerprint



Power button board

